

From: tbr
Sent: Thursday, September 01, 1994 12:12 AM
To: 'tbe@MicroUnity.com'
Cc: 'al'; 'graham'; 'h'; 'jt'; 'mouss'; 'noel'; 'philip'
Subject: Power/size
Follow Up Flag: Follow up
Flag Status: Red

tbe@MicroUnity.com wrote (on Wed Aug 31):

Hi,

Given the growth in Hestia total power consumption, and the consequent growth in size (reflected in the design reviewed on 8/9), I would like to suggest a course of action to ensure that an acceptable power consumption level and product size is obtained before too long (before we find ourselves in an adverse competitive situation).

1) Pursue synchronous rectification aggressively.

We have been unable to find an off-the-shelf 3.3V dc-dc converter with better than ~76% efficiency. The RO dc-dc unit we are using has been optimized to this efficiency, and the consequence for Hestia is a power supply dissipation of ~50 Watts (when it is delivering to the ~36 amp load for 3.3V, along with the 12V and 5V dc loads described in the design review). This corresponds to a worst-case steady state unit dissipation of ~200W.

IBM has described (sorry, I forget the ref.) a 3.3V dc synchronous rectifier based supply with >90% efficiency. Motorola has described 3A supplies at 3.3V available now. Other schemes such as the ~90% efficient 50(?)A 3.3V supply described in a Maxim application note are worthy of further investigation. I surely do not know the latest in power supply technology, but it seems to me we should at least become closely tied in to the leaders in this area.

I acknowledge that this approach will not result in the lowest cost per Watt for a while, but I am assuming a) that MicroUnity's chips will often involve relatively high power consumption for the next several years and b) that total product cost will not be as critical as power consumption for the trials. Therefore competitive forces will tend to put a premium on greater efficiency in the off-chip functions. This is especially true with wireless, battery powered products. If we simply pursue the cheapest open frame (~\$.15/Watt) supplies, we will have inherently higher power consumption (not to mention larger products!), and will not have anticipated the inevitable emergence of synchronous rectification and other highly efficient power conversion technologies. We will also be behind on working their price curves down. Of course, a concerted effort and some production volume (such has been discussed for late 1995) is necessary to successfully incorporate advanced technology power supplies.

Long ago, when the original "brick" mockup was constructed we discussed the possibility of integrating the control circuitry for

a switching power supply onto one of our chips. The motivation at that time was cost reduction to eliminate external components. However, we rejected the idea on the grounds that there was additional risk and the cost savings would be minimal given that the bulk of the PSU cost was in the magnetics. I'm not familiar with the details of synchronous rectification, but if there is a way to make it more cost effective by exploiting the availability of a large number of active devices in a small area of our silicon it would be worth investigation.

2) Develop near unity power factor ac-dc circuit.

The power factor of the current Hestia design is $\sim .5$. Therefore, the power consumption in VA is over 400 VA. This seems untenable for a high volume product, and is unsellable in Europe. Can we agree that this is a priority for a high volume product?

3) Implement power reduction techniques on Calliope and Euterpe.

As soon as the first Calliope and Euterpe revisions are functional, should we not at some point in the near future put together a team to further investigate, develop, and implement power reduction techniques? If this only saves 5% per chip, it seems to me to be worth a dedicated effort, because even with a $>90\%$ efficient power supply (including the inevitable 98% efficient ac-dc converter), total unit power is $\sim 180W$ with current Calliope/Euterpe power levels (55 and 65 Watts respectively) and the other power consumers in the BOM.

This is not isolated from the supply efficiency issue because one of the main ideas we have investigated for power reduction would involve dropping the supply to around 1.7V. This is much less attractive if we then just take another hit in supply efficiency.

I do not mean to suggest that we change course on the first prototype of Hestia we are all working on, even though I among others wish it were smaller, cooler, etc. Not that the schedule could stand it anyway, and I believe that we will learn much of value (what RF front end architecture is best, what components go away, etc.) that is necessary to know before spending more resources on the power supply. Then we can rapidly develop products for lower total power as needed.

To be concrete, what I suggest is that as soon as the first Hestia protos are complete, a power supply "champion" should be identified, and that person should address items 1 and 2 above. In the meantime, it seems to me to be worthwhile for procurement (Wamaitha), working from a minimal spec, to identify potential sources or partners for high efficiency 3.3V power supplies. Regarding Calliope and Euterpe, we've often discussed future power reduction strategies; what I'm not qualified to say is when these should be jumped on.

I know I'm not the only one who has seen products suffer due to less effort being expended on the power subsystem than on the primary functional components, so I hope nobody minds my message here. I also acknowledge that much effort has been expended to get the RO to the current efficiency. My intent is to get a consensus going for the next year or so; up until now, power supplies ranging from the el cheapo open frame type to exotic synchronous rectifiers have been proposed, just as for Calliope and Euterpe I've heard everything from further power reduction being highly unlikely to obtaining 4X power reduction for high volume discussed. If we are to obtain a product close in size to the model made in April, we need to make some decisions now, I believe.

There is definitely scope for reduction, though I've never heard anyone go so far as 4X, certainly not without a substantial reduction in performance/functionality. Currently our focus is on getting an implementation as quickly as we can and there is no way we should delay that to reduce power in the first version. The recent change in cell family (which does reduce power 10-15% for given functionality) was done to reduce area in order that we can get the functionality we need on the die. We don't see any overall power saving because of course the saved area is taken up with additional circuitry.

Please let me know your thinking in this matter.

Tim

.

From: tbe@MicroUnity.com
Sent: Thursday, September 01, 1994 1:22 AM
To: 'Tim B. Robinson'
Subject: Re: Power/size

>
>Long ago, when the original "brick" mockup was constructed we
>discussed the possibility of integrating the control circuitry for
>a switching power supply onto one of our chips. The motivation at
>that time was cost reduction to eliminate external components.
>However, we rejected the idea on the grounds that there was additional
>risk and the cost savings would be minimal given that the bulk of the
>PSU cost was in the magnetics. I'm not familiar with the details of
>synchronous rectification, but if there is a way to make it more cost
>effective by exploiting the availability of a large number of active
>devices in a small area of our silicon it would be worth
>investigation.
>
>snip<
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>98% efficient ac-dc converter), total unit power is ~180W with current
>Calliope/Euterpe power levels (55 and 65 Watts respectively) and the other
>power consumers in the BOM.
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>This is not isolated from the supply efficiency issue because one of
>the main ideas we have investigated for power reduction would involve
>dropping the supply to around 1.7V. This is much less attractive if
>we then just take another hit in supply efficiency.
>

You're so right--in one discussion with Mouss about this, he suggested that
it would be necessary to have the level converters on-chip, at least for
the mixed-signal chip, in order to have the higher voltage for the analog
stuff. What would this involve? Is it something you've looked at before?

>snip<
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>go so far as 4X, certainly not without a substantial reduction in
>performance/functionality. Currently our focus is on getting an
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>course the saved area is taken up with additional circuitry.
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> Please let me know your thinking in this matter.
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Thanks for your comments. I agree of course with your statement that we can't delay--I feel somewhat useless in this matter due to my mechanical pedigree. I hope those who do seem to understand synchronous rectification (Noel, Al(?)) will respond. Do you think it would be fruitful to generate an envelope spec. and have Wamaitha do some research on suppliers with Noel (when available) for technical support?

Tom Eich tbe@microunity.com
MicroUnity Systems Engineering, Inc.
255 Caspian Dr. Sunnyvale, CA 94089
(408)734-8100, (408)734-8136 fax

From: tbr
Sent: Thursday, September 01, 1994 3:42 PM
To: 'tbe@MicroUnity.com'
Subject: Re: Power/size
Follow Up Flag: Follow up
Flag Status: Red

tbe@MicroUnity.com wrote (on Wed Aug 31):

>
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>that time was cost reduction to eliminate external components.
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>PSU cost was in the magnetics. I'm not familiar with the details of
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You're so right--in one discussion with Mouss about this, he suggested that it would be necessary to have the level converters on-chip, at least for the mixed-signal chip, in order to have the higher voltage for the analog stuff. What would this involve? Is it something you've looked at before?

We (that is bill herndon) have looked in some depth at a logic family operating off 1.7. It also requires a rail one logic swing (about 0.5V below the upper rail. No-one has looked seriously into how to provide those rails efficiently. In this family, the logic itself is running off the 1.7, but the wire drivers effectively switch 0.5V into the heavy loads. So if there is a way to get .5V efficiently we have a real win. If we get it by dumping the rest of the 1.7V rail, then the best we can expect is order 50% reduction from the 3.3 -> 1.7 change.

>snip<

>

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>go so far as 4X, certainly not without a substantial reduction in

>performance/functionality. Currently our focus is on getting an

>implementation as quickly as we can and there is no way we should

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>Tim

Thanks for your comments. I agree of course with your statement that we can't delay--I feel somewhat useless in this matter due to my mechanical pedigree. I hope those who do seem to understand synchronous rectification (Noel, Al(?)) will respond. Do you think it would be fruitful to generate an envelope spec. and have Wamaitha do some research on suppliers with Noel (when available) for technical support?

I've got the impression (and I have no real knowledge here) that this is really still a research area. However, much of the rest of what we are doing is at the frontiers of research right now, so that alone should not stop us from pursuing it. The main obstacle is perhaps not having the right skills on board. If we made a strategic decision that this was an essential technology to develop, I don't see why we should be afraid to mount the effort.

Tim

From: sysadm@gaea on behalf of Guillermo A. Loyola [gmo@microunity.com]
Sent: Thursday, September 01, 1994 7:37 PM
To: 'euterpe@gaea'

This is it! With tonight's builds we will be switching 1) to the new opcodes, and 2) to little endian tools in /a/soft/stb/bin.

Change #1 means that all of your terp code will be incompatible and you'll need to clobber and recompile. The new-opcode tools *have* been used to build the whole stb tree and all the diagnostics, tests and the benchmark work.

Change #2 means that if you are using big-endian tools and using /a/soft/stb/bin in your path, you should change to /a/soft/bstb/bin (if you haven't done that, you can do it now; as there are already links that point to the "right places"); and if you are a user of the little-endian tools and have either /a/soft/lstb/bin or /a/soft/nstb/bin in your path (or Makerules.local), tomorrow you should change those to be /a/soft/stb/bin.

I'm going to start checking in the changes now, and I'll change the /a/soft/stb link as close as possible to 10pm. As many of you know the builds start at 8pm (BE sgi), 9pm (BE sun), 10pm (LE sgi) and 11pm (LE sun); so assuming it all works the corresponding binaries/libraries/includes should be in place about an hour after the start of the build. If things go wrong I'll try to fix them and start new builds asap.

Let me know if you have any problems.

Gmo.

From: Tim B. Robinson [tbr@demeter]
Sent: Thursday, September 01, 1994 9:44 PM
To: 'Bob Morgan'
Cc: 'euterpe@demeter'
Subject: NB cerberus bits

Bob Morgan wrote (on Thu Sep 1):

Hi,
Did anyone ever decide which 4 bits in which
Cerberus register will define how many of the
NB entries can be consumed by low priority
requests?

No, but gmo suggested 48-52 and I think that looks like a good choice.
It allows room for expansion to a larger NB in a future implementation. Lets go with
that.

Tim

From: Mark Hofmann [hopper@cyclops]
Sent: Friday, September 02, 1994 6:09 AM
To: 'vant'
Cc: 'orlando@hestia'; 'vanthof@hestia'; 'geert@hestia'; 'hopper@hestia'; 'vo@hestia'
Subject: Re: baseplate upper drc job finished

vant sez:

The upper drc's finished for the baseplate and it's about 722kb in size.

It's location is

/u/vanthof/compass/mobi/euterpe/baseplate_upper.err

Thanks,
Dave

It looks like about 3/4th of the errors are "offgrid". The rest are width/space and cover errors.

-hopper

From: vant [vanthof@hestia]
Sent: Friday, September 02, 1994 12:56 PM
To: 'Orlando Hernando'
Cc: 'Dave Van't Hof'; 'Geert Rosseel'; 'Mark Hofmann'; 'Tom Vo'
Subject: baseplate upper drc job finished

The upper drc's finished for the baseplate and it's about 722kb in size.

It's location is

/u/vanthof/compass/mobi/euterpe/baseplate_upper.err

Thanks,
Dave

--
Dave Van't Hof vanthof@microunity.com MicroUnity Systems Engineering,
Inc.
"What rolls down stairs, alone or in pairs, rolls over the neighbor's dog?"

What's great for a snack and fits on your back? It's log, log, log!"
LOG from BLAMMO! (tm) All kids love Log! #include
<std_disclaim.h>

From: Eldred Felias [efelias@poseidon]
Sent: Friday, September 02, 1994 3:06 PM
To: 'B. P. Wong'
Cc: 'Geert Rosseel'
Subject: Output from "at" job (fwd)

BP,

Here is the output for cr (ran on iss). It's clean.

```
Eldred
=====
Forwarded message:
>From root@tomato Fri Sep  2 12:40:32 1994
>Date: Fri, 2 Sep 1994 12:40:30 -0700
>From: root@tomato (Charlie Root)
>Message-Id: <199409021940.MAA28742@tomato.microunity.com>
>To: efelias@tomato
>Subject: Output from "at" job
>
>Your "at" job "2002" produced the following output:
>
>
>Working cell: cr
>Using flow: /u/chip/technology/mobimos/iss//mobilvsl_p611.vc
>Translation table for Cif To Stream:
/u/chip/tools/lib/stream/mobimos1.tbl
>
>Current working directory: /usr/local/etc/dracjobs/isslvs Current
>Layout: cr
>rm: cannot remove `.' or `..'
>rm: cannot remove `.' or `..'
>
>LTLPTH:      /a/iss
>ISSPATH:     /a/iss
>ISS_SYSTYPE: SUN4
>ISS_LSERVER: hestia
>
>/a/iss/SUN4_verichk/vc_engine
>
>/*****/
> *
> *          IIIIIII  SSSSSS  SSSSSS  *
> *            I      S      S      *
> *            I      S      S      *
> *            I      SSSSS  SSSSS  *
> *            I      S      S      *
> *            I      S      S      *
> *          IIIIIII  SSSSSS  SSSSSS  *
> *
>/*****/
>
>cdl2iss.pl
>Parsing /n/auspex/s9/efelias/vlsir/euterpe/cr.sp
>Creating schematic.iss.tmp
>Creating cell.equiv
>
>UNWIRE Hierarchical Netlist Wire Remover - Version BETA 1.7   3/10/94
>Copyright (C) Integrated Silicon Systems 1991-1993. All rights reserved.
>
>Creating composite LVS explode and flatten lists
```



```

>
>Starting date:   Fri Sep  2 11:41:25 PDT 1994
>
>/u/chip/tools/bin/cifles -c cr -v
/n/auspex/s9/efelias/vlsiir/euterpe/vlsi.boo -o 28299.cif -h cell.equiv -I
n 28299.txt -e 1 -Y -G BBOX  >>& cr.log
>/u/chip/tools/bin/ciftostm -I 28299.cif -O datain.dat -X
/u/chip/tools/lib/stream/mobimos1.tbl -h
>Translation of 28299.cif succeeded.
>Root symbol is called ROOTCELL.
>Running vericheck
>   gdsin: 5.1.2 6/22/94
>   gdsout: 5.1.8 6/6/94
>   herc: 2.4.2 7/21/94
>   lsh: 2.4.15 8/18/94
>   vc_engine: 2.4.122 8/30/94
>   vp: 2.4.17 7/11/94
>VeriCheck is done.
>
>VeriCheck (R) Hierarchical Design Verification, BETA 2.4.1
> (C) Copyright 1990, 1991, 1992, 1993, 1994.
> Integrated Silicon Systems, Inc. All rights reserved.
> This product contains confidential information and trade secrets of
> Integrated Silicon Systems, Inc. Any use or disclosure, except as
> authorized in writing by Integrated Silicon Systems, Inc., is
> prohibited. Copyright is claimed in this product as an unpublished
> work, and the copyright notice does not imply publication.
>
>Printing individual version numbers ...
>
>   vericheck: 2.4.9 8/24/94
>
>
>Check following files for results:
>   Error File = "CR.cmperr"
>   Summary File = "CR.cmpsum"
>
>herc [options] <Netlist> <Runset>
>   -e <file> : Redirect error messages to error file
>   -n# : Set net size limit when printing connections
>   -b <block> : Set block
>   -r <root> : Set root cell
>   -s <file> : Redirect log messages to summary file
>   -z : Print nets with zero connections
>
>Check following files for results:
>   Error File = "CR.ercerr"
>   Summary File = "CR.ercsum"
>
>VeriCheck is done.
>
>*****
>*          Compare summary          *
>   CRCELL#1 == CRCELL
>   CRRDEC1 == CRRDEC1
>   CRBBCSTM == CRBBCSTM
>   CRSASPLAT == CRSASPLAT
>   CROR2WP == CROR2WP
>   CRADDMPL == CRADDMPL
>   CRWEPLAT == CRWEPLAT
>   CRGSA == CRGSA
>   CRDDRV == CRDDRV
>   CRLOCSA == CRLOCSA
>   CRDINMPL == CRDINMPL
>   CRSDRV == CRSDRV
>   CRXDRV == CRXDRV
>   CRDINDRV == CRDINDRV
>   CRBELLYBUTT == CRBELLYBUTT

```

```

> CRDSPLAT == CRDSPLAT
> CRWEDRV == CRWEDRV
> CRXDRV == CRXDRV
> CRSELEF == CRSELEF
> CRASEF == CRASEF
> CRSELEFP == CRSELEFP
> CRPRE8 == CRPRE8
> CRLSA32C == CRLSA32C
> CRPRE4 == CRPRE4
> CR3PGSA == CR3PGSA
> CRRDEC == CRRDEC
> CR1COL == CR1COL
> CR8COL == CR8COLR
> CR8COL == CR8COL
> CR16COL == CR16COLR
> CR16COL == CR16COL
> CR64COL == CR64COL
> CR64COL == CR64COLR
> CRARRAY == CRARRAY
> CR3A == CR3A
> CR2A == CR2A
> CR == CR
> CRCELL#1 == CRCELL (level 8)
> CRRDEC1 == CRRDEC1 (level 8)
> CRBBCSTM == CRBBCSTM (level 8)
> CRSASPLAT == CRSASPLAT (level 8)
> CROR2WP == CROR2WP (level 8)
> CRADDMPL == CRADDMPL (level 8)
> CRWEPLAT == CRWEPLAT (level 8)
> CRGSA == CRGSA (level 8)
> CRDDRV == CRDDRV (level 8)
> CRLOCSA == CRLOCSA (level 8)
> CRDINMPL == CRDINMPL (level 8)
> CRDSDRV == CRDSDRV (level 8)
> CRXDRV == CRXDRVR (level 8)
> CRDINDRV == CRDINDRV (level 8)
> CRBELLYBUTT == CRBELLYBUTT (level 8)
> CRDSPLAT == CRDSPLAT (level 8)
> CRWEDRV == CRWEDRV (level 8)
> CRXDRV == CRXDRV (level 8)
> CRSELEF == CRSELEF (level 8)
> CRASEF == CRASEF (level 8)
> CRSELEFP == CRSELEFP (level 8)
> CRPRE8 == CRPRE8 (level 7)
> CRLSA32C == CRLSA32C (level 7)
> CRPRE4 == CRPRE4 (level 7)
> CR3PGSA == CR3PGSA (level 7)
> CRRDEC == CRRDEC (level 6)
> CR1COL == CR1COL (level 6)
> CR8COL == CR8COLR (level 5)
> CR8COL == CR8COL (level 5)
> CR16COL == CR16COLR (level 4)
> CR16COL == CR16COL (level 4)
> CR64COL == CR64COL (level 3)
> CR64COL == CR64COLR (level 3)
> CRARRAY == CRARRAY (level 2)
> CR3A == CR3A (level 1)
> CR2A == CR2A (level 1)
> CR == CR (level 0)
> *****
>
> *****
> *****
> **
> **   THERE ARE OPENS IN YOUR CIRCUIT   **
> **   PLEASE LOOK IN CR.err             **
> **                                     **

```

```

>*****
>*****
>
>mv CR.sum CR.err CR.cmpsum CR.cmperr CR.net CR.ercsum CR.ercerr CR.tree
schematic.iss cell.equiv edtext.dat compare
>mv: CR.ercsum: Cannot access: No such file or directory
>mv: CR.ercerr: Cannot access: No such file or directory cp -rp compare/
>/n/auspex/s9/efelias/vlsir/euterpe/cr.compare
>cp: compare//.matched/CRCELL: No such file or directory
>cp: compare//.matched/CRRDEC1: No such file or directory
>cp: compare//.matched/CROR2WP: No such file or directory
>cp: compare//.matched/CRADDMPL: No such file or directory
>cp: compare//.matched/CRWEPLAT: No such file or directory
>cp: compare//.matched/CRGSA: No such file or directory
>cp: compare//.matched/CRDDRV: No such file or directory
>cp: compare//.matched/CRLOCSA: No such file or directory
>cp: compare//.matched/CRDINMPL: No such file or directory
>cp: compare//.matched/CRSDRV: No such file or directory
>cp: compare//.matched/CRXDRV: No such file or directory
>cp: compare//.matched/CRDINDRV: No such file or directory
>cp: compare//.matched/CRDSPLAT: No such file or directory
>cp: compare//.matched/CRWEDRV: No such file or directory
>cp: compare//.matched/CRXDRV: No such file or directory
>cp: compare//.matched/CRSELEF: No such file or directory
>cp: compare//.matched/CRASEF: No such file or directory
>cp: compare//.matched/CRSELEFP: No such file or directory
>cp: compare//.matched/CRLSA32C: No such file or directory
>cp: compare//.matched/CRPRE4: No such file or directory
>cp: compare//.matched/CR3PGSA: No such file or directory
>cp: compare//.matched/CR1COL: No such file or directory
>cp: compare//.matched/CR8COLR: No such file or directory
>cp: compare//.matched/CR8COL: No such file or directory
>cp: compare//.matched/CR16COLR: No such file or directory
>cp: compare//.matched/CR16COL: No such file or directory
>cp: compare//.matched/CR64COL: No such file or directory
>cp: compare//.matched/CR64COLR: No such file or directory
>cp: compare//.matched/CRARRAY: No such file or directory
>cp: compare//.matched/CR: No such file or directory cat cr.log >>
>/n/auspex/s9/efelias/vlsir/euterpe/cr.compare/cr.lvslog
>
>ISS LVS completed
>
>

```

--

.

From: tbr
Sent: Friday, September 02, 1994 11:11 PM
To: 'woody'
Subject: gt
Follow Up Flag: Follow up
Flag Status: Red

I get this warning from v2e when compiling the top level:
Translating Verilog source

(?V2E) ***WARNING*** Illegal port connection on Port "ibWe_N[0]" of instance "gt" of module "gt"
Writing output to tbr3_euterpe.v2e

I think it's a floating inverting input (which topt would tie to
vref). is this intended? (BOM 107)

Tim

.

From: Lisa Robinson [lisar@rhodan]
Sent: Friday, September 02, 1994 11:13 PM
To: 'cadettes@rhodan'
Cc: 'jeffm@rhodan'; 'mws@rhodan'; 'sysadm@rhodan'; 'tbr@rhodan'
Subject: nosferatu

The VXI license has expired and I can't build a euterpe edif netlist for zycad simulation.

Could someone please set the date on nosferatu to August 25th.

Many thanks.

Lisa R.

.

From: tbr
Sent: Saturday, September 03, 1994 1:26 AM
To: 'hopper'
Subject: ea cell
Follow Up Flag: Follow up
Flag Status: Red

topt is reporting:

Reading Legal Cell List file /n/auspex/s15/tbr/euterpe/proteus/exlax/toptList
ReadLegalCellFile: Warning! No atoms info for eawdr5ffnf4s3x4a

(this on a design with no exlax arrays).

Tim

.

From: tbr
Sent: Saturday, September 03, 1994 2:11 AM
To: 'woody'
Cc: 'mws'
Subject: gt
Follow Up Flag: Follow up
Flag Status: Red

There is definitely something wrong with gt (BOM 107). Besides the previous undriven net I found I also get this warning at the top level from v2e:

"tbr3_euterpe.v", 1906: warning! port sizes differ in port connection (port 71)
"tbr3_euterpe.v", 1906: warning! port sizes differ in port connection (port 72)

1906 is the gt instantiation.

Tim

.

From: Mark Hofmann [hopper@boreas]
Sent: Saturday, September 03, 1994 9:37 PM
To: 'Tim B. Robinson'
Cc: 'Brian Lee'; 'vant@boreas'
Subject: Re: ea cell

Tim B. Robinson sez:

topt is reporting:

Reading Legal Cell List file /n/auspex/s15/tbr/euterpe/proteus/exlax/toptList
ReadLegalCellFile: Warning! No atoms info for eawdr5ffnf4s3x4a

(this on a design with no exlax arrays).

Hmm. I'm a little confused on this one. /u/chip/proteus/exlax/toptList _does_ mention eawdr5ffnf4s3x4a but the Makefile in elibsrc looks like it ought no longer to produce any eawdr* type cells (the new clock scheme has Exlax switching over to ealpor!* cells). Perhaps a make clean is in order?

-hopper

.

From: tbr
Sent: Saturday, September 03, 1994 9:40 PM
To: 'Mark Hofmann'
Cc: 'Brian Lee'; 'vant@boreas'
Subject: Re: ea cell
Follow Up Flag: Follow up
Flag Status: Red

Mark Hofmann wrote (on Sat Sep 3):

Tim B. Robinson sez:

topt is reporting:

Reading Legal Cell List file /n/auspex/s15/tbr/euterpe/proteus/exlax/toptList
ReadLegalCellFile: Warning! No atoms info for eawdr5ffnf4s3x4a

(this on a design with no exlax arrays).

Hmm. I'm a little confused on this one. /u/chip/proteus/exlax/toptList _does_ mention cawdr5ffnf4s3x4a but the Makefile in elibsrc looks like it ought no longer to produce any eawdr* type cells (the new clock scheme has Exlax switching over to ea1porl* cells). Perhaps a make clean is in order?

probably worth it if we think everything is otherwise stable.

Tim

.

From: Jay Tomlinson [woody@pegasus]
Sent: Saturday, September 03, 1994 10:54 PM
To: 'Tim B. Robinson'
Subject: gt

Tim B. Robinson wrote (on Fri Sep 2):

I get this warning from v2e when compiling the top level:
Translating Verilog source

(?V2E) ***WARNING*** Illegal port connection on Port "ibWe_N[0]" of instance "gt" of module "gt"
Writing output to tbr3_euterpe.v2e

I think it's a floating inverting input (which topt would tie to
vref). is this intended? (BOM 107)

Tim
No this is not intended. This is from a pla. I will look at see if I see
anything wrong.

Jay

.

From: tbr
Sent: Saturday, September 03, 1994 11:21 PM
To: 'Jay Tomlinson'
Cc: 'billz@nosferatu'; 'dickson@nosferatu'; 'Lisa Robinson'; 'mws@nosferatu'
Subject: BOM108
Follow Up Flag: Follow up
Flag Status: Red

Jay Tomlinson wrote (on Sat Sep 3):

Lisa Robinson wrote (on Fri Aug 26):

So far 3 tests have failed, gtlb, exmaskeasy and store.

(The store looks like one cylinder got it wrong! I'll point you at a dump later).

I have been trying to figure out why gtlb fails. It runs okay in verilog both with the real and behavioral gtlb. However I do get the message:

Warning! Port sizes differ in port connection (port 26) [Verilog-PCDPC]
"gt/gt.v", 86: snakeAddr

Warning! Port sizes differ in port connection (port 27) [Verilog-PCDPC]
"gt/gt.v", 86: snakeAddr_N

When I compile. I can't find the difference though - I've looked pretty hard!

Lisa R.

In gt.V I define snakeAddr as 47:0, but I actually only drive 10:5. Could this cause the problem?

Should be OK if there is nothing connected to the other bits. But if something else is hooked to them we will have floating inputs.

Tim

.

From: vant [vanthof@hestia]
Sent: Sunday, September 04, 1994 11:39 AM
To: 'Tim B. Robinson'
Cc: 'hopper@boreas'; 'vant@boreas'
Subject: Re: new Planet, T2pla, Plat being installed

Tim B. Robinson writes:

>
>
>I found there was another tmp file specified on the command line that
>was not unique. I fixed that. Even if the cells were unique, we
>always as a precaution remove the xshadowx before it starts, so of
>course one run clobbers another there. And, in this case I was in the
>ged/pl directory compiling the plls, which do share common sub cells,
>so there'd probably be trouble from that.
>
>Tim
>

The approach we took at mips was to have a common xshadowx location for every job on a disk accessible to everyone. This had two affects:

- compiles were significantly faster since the compiler only had to check for things out of date and recompile those
- disk space savings as there were no redundant xshadowx directories lying around.

An approach we might want to look into is to have a common xshadowx directory for each 'chip'. such as one for euterpe, calliope, proteus, etc. That way if someone has a local copy of euterpe, but references the common proteus, the only things getting compiled would be for the local euterpe. This does have a disk space impact as these directories would need to be left around.

Anyway, just a thought.
Dave

--
Dave Van't Hof vanthof@microunity.com MicroUnity Systems Engineering, Inc.
"What rolls down stairs, alone or in pairs, rolls over the neighbor's dog?
What's great for a snack and fits on your back? It's log, log, log!"
LOG from BLAMMO! (tm) All kids love Log! #include <std_disclaim.h>

From: tbr
Sent: Sunday, September 04, 1994 1:00 PM
To: 'vant'
Cc: 'hopper@boreas'; 'vant@boreas'
Subject: Re: new Planet, T2pla, Plat being installed
Follow Up Flag: Follow up
Flag Status: Red

vant wrote (on Sun Sep 4):

Tim B. Robinson writes:

```
>
>
>I found there was another tmp file specified on the command line that
>was not unique. I fixed that. Even if the cells were unique, we
>always as a precaution remove the xshadowx before it starts, so of
>course one run clobbers another there. And, in this case I was in the
>ged/pl directory compiling the plis, which do share common sub cells,
>so there'd probably be trouble from that.
>
>Tim
>
```

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- compiles were significantly faster since the compiler only had to check for things out of date and recompile those
- disk space savings as there were no redundant xshadowx directories lying around.

An approach we might want to look into is to have a common `xshadowx` directory for each 'chip'. such as one for euterpe, calliope, proteus, etc. That way if someone has a local copy of euterpe, but references the common proteus, the only things getting compiled would be for the local euterpe. This does have a disk space impact as these directories would need to be left around.

Anyway, just a thought.

My understanding was that removing the xshadowx was not to save disk space, but rather because the compiler was not always reliable in deciding when to recompile.

Tim

.

From: Richard Dickson [dickson@demeter]
Sent: Sunday, September 04, 1994 1:36 PM
To: 'tbr@demeter'
Subject: es placement

tim,

i've updated everything that you suggested but it still
doesn't work for me. see .. dickson/euterpe/verilog/bsrc/es/aaa

that my log file of my last 'gmake esgards'

cgcclockbias is not placing for some reason. all the es parts place ok tho.

dickson

.

From: tbr
Sent: Sunday, September 04, 1994 1:37 PM
To: 'Richard Dickson'
Subject: es placement
Follow Up Flag: Follow up
Flag Status: Red

Richard Dickson wrote (on Sun Sep 4):

tim,

i've updated everything that you suggested but it still
doesn't work for me. see .. dickson/euterpe/verilog/bsrc/es/aaa

that my log file of my last 'gmake esgards'

egcclockbias is not placing for some reason. all the es parts place ok tho.

OK, looking now.

Tim

.

From: tbr
Sent: Sunday, September 04, 1994 1:46 PM
To: 'Richard Dickson'
Subject: es placement
Follow Up Flag: Follow up
Flag Status: Red

Richard Dickson wrote (on Sun Sep 4):

tim,

i've updated everything that you suggested but it still
doesn't work for me. see .. dickson/euterpe/verilog/bsrc/es/aaa

that my log file of my last 'gmake esgards'

cgcclockbias is not placing for some reason. all the es parts place ok tho.

First, please update verilog/bsrc/pimlib.pl.

There is something odd about the dates:

```
208 -rw-r--r-- 1 dickson 198747 Sep 3 18:15 es-pass1.pim
208 -rw-r--r-- 1 dickson 198747 Sep 3 18:16 es.pim
  1 -rw-r--r-- 1 dickson 632 Sep 3 15:51 genpim.pl
  1 -rw-r--r-- 1 dickson 433 Sep 3 15:51 pimlib.pl
```

See how es-pass1.pim looks older than es.pim? The log does not show
es-pass1.pim getting generated at all. I found a missing dependency
in the es/Makefile (as a result of the change I made, sorry). It must
have worked for me because I had a clean start. I checked in a new
Makefile in es. Please update that too and run again.

Sorry for the hassle.

Tim

From: Tim B. Robinson [tbr@aphrodite]
Sent: Sunday, September 04, 1994 1:52 PM
To: 'geert@aphrodite'
Cc: 'brianl@aphrodite'; 'vanthof@aphrodite'
Subject: custom timing file

I am still seeing:

Unknown fanin 1 intrinsic delay sc1p3 in
/n/auspex/s15/tbr/euterpe/proteus/custom/time/tim.lib at line 67 Unknown fanin 1 intrinsic
delay sc1p3 in /n/auspex/s15/tbr/euterpe/proteus/custom/time/tim.lib at line 72 Unknown
fanin 1 intrinsic delay sc1p3 in /n/auspex/s15/tbr/euterpe/proteus/custom/time/tim.lib at
line 77 Unknown fanin 1 intrinsic delay sc1p3 in
/n/auspex/s15/tbr/euterpe/proteus/custom/time/tim.lib at line 82

.

From: tbr
Sent: Sunday, September 04, 1994 2:27 PM
To: 'vanthof'
Subject: Possible topt problem
Follow Up Flag: Follow up
Flag Status: Red

I am getting complaints from slnet of the form:

(* 14334 *) RG/RGPC/UPCPLR1/U23.Q_AD0PH, RG/RGPC/UPCPLR2/U23.D0_ADMPH,
[EUTERPE]

^
** SDL Parser Error 8 ** Symbol pin not defined on the logic description.

(* 14395 *) RG/RGPC/UPCPLR1/U15.Q_AD0PH, RG/RGPC/UPCPLR2/U15.D0_ADMPH,

^
** SDL Parser Error 8 ** Symbol pin not defined on the logic description.

(* 14861 *) RG/RGPC/UPCPLR1/U47.Q_AD0PH, RG/RGPC/UPCPLR2/U47.D0_ADMPH,

^
** SDL Parser Error 8 ** Symbol pin not defined on the logic description.

I believe these may be the very gates that you had to deal with where the sub block says make them full swing, then at the top level after pruning they become half swing. The output pin names may be gatting written out in correctly. I do notice the following in the sdl file (note lowe case 'h') but I think it's unrellated, because the cells in question should be xbff's of ome sort, not xbfte's.

```
NAME: xbfedh2s;
TYPES: ;
EXT:: phi_a2p1c, phi_b2p1c, phi_a2p2c, phi_b2p2c, D0_ADMPH, D0_ANDMPH,
      Q_AD1Ph, Q_AND1Ph;
INPUTS: .phi_a2p1c, .phi_b2p1c, .phi_a2p2c, .phi_b2p2c, .D0_ADMPH,
      .D0_ANDMPH;
OUTPUTS: .Q_AD1Ph, .Q_AND1Ph;
END;
ENDC;
```

The evidence is in my bsrc/gards/tbr2_euterpe.....

Tim

.

From: tbr
Sent: Sunday, September 04, 1994 2:36 PM
To: 'vanthof'
Subject: topt problem
Follow Up Flag: Follow up
Flag Status: Red

OK. Loads of confusion. The relevant .sld file is
bsrc/gards/tbr2_euterpe-iter.sdl. The relevant info is:

```
xbffd6s:    rg/rgpc/UpcPIR1/u39, rg/rgpc/UpcPIR1/u23,  
            rg/rgpc/UpcPIR1/u15, rg/rgpc/UpcPIR1/u7, rg/rgpc/UpcPIR1/u3,  
            rg/rgpc/UpcPIWQ/u62, rg/rgpc/UpcPIWQ/u61, rg/rgpc/UpcPIWQ/u60;  
  
rg/rgpc/pcPIR1<23>(PINCAPACITANCE="",RESISTANCE="",CAPACITANCE="")=  
            rg/rgpc/UpcPIR1/u23.Q_AD0PH, rg/rgpc/UpcPIR2/u23.D0_ADMPH,  
            rg/rgpc/UpcPIIncR1/Uinc2/Us/u7.D0_AD0PH,  
            rg/rgpc/UpcPIIncR1/Uinc2/Us/u7.D1_AND0PH;
```

ie it's a full swing gate, yet the netlist section calls out an AD0PH
output pin name.

Tim

.

From: vant [vanthof@hestia]
Sent: Sunday, September 04, 1994 4:27 PM
To: 'Tim B. Robinson'
Cc: 'vanthof@aphrodite'
Subject: Re: topt problem

Tim B. Robinson writes:

>
>
>OK. Loads of confusion. The relevant .sld file is
>bsrc/gards/tbr2_euterpe-iter.sdl. The relevant info is:

Well, I'm back on line. We just got back and I'll take a look at this.

Thanks,
Dave

—
Dave Van't Hof vanthof@microunity.com MicroUnity Systems Engineering, Inc.
"What rolls down stairs, alone or in pairs, rolls over the neighbor's dog?
What's great for a snack and fits on your back? It's log, log, log!"
LOG from BLAMMO! (tm) All kids love Log! #include <std_disclaim.h>

From: Tom Vo [vo@merope]
Sent: Tuesday, September 06, 1994 12:49 PM
To: 'Tom Laidig'
Cc: 'vanthof@hestia'; 'solo@clio'; 'bpw@clio'; 'lisar@clio'; 'tbr@clio'; 'cadettes@clio'; 'tom@clio'; 'vo@clio'; 'geert@clio'
Subject: Re: ctag and cr metal 5

Tom Laidig wrote

>I agree that this should be checked, but I think this is a real
>error. Unless the rules have been changed since I last heard, custom
>blocks are supposed to be multiples of 24u, and they're supposed to be
>placed on multiples of 24u, so we can be sure there's an obvious way
>for

I did not know about this rule . The rule I've been using for both calliope and euterpe .

In the x direction , place on 4u grid
In the y direction , place on 24u grid

If a cell is intended to be rotated when placed , then both its x and y dimensions has to
be a multiple of 24u .

tvo

From: Geert Rosseel [geert@ambiorix]
Sent: Tuesday, September 06, 1994 2:20 PM
To: 'fwo@pelagon'; 'tom@clio'; 'vo@merope'
Cc: 'bpw@clio'; 'cadettes@clio'; 'geert@clio'; 'lisar@clio'; 'solo@clio'; 'tbr@clio'; 'vanthof@hestia'
Subject: Re: ctag and cr metal 5

>To greatly simplify the assembly process, Geert has had the layout
>staff
place
> M5 on a 24um by 24um grid so that layouts could be placed in any
orientation.

Hi,

I don't think the above is true. We are still living by the rules that Tom Vo mentioned :
4U in X and 24 u in Y except for blocks that will get rotated which need 24u spacing on
all sides. On calliope, most blocks were analog blocks and since we did not know their
orientation, we defaulted to 24 on all sides

On Euterpe, I believe most blocks follow the 24x24 rules, but the register file does not.

Geert

From: Fred Obermeier [fwo@pelagon]
Sent: Tuesday, September 06, 1994 2:41 PM
To: 'geert@ambiorix'; 'tom@clio'; 'vo@merope'
Cc: 'bpw@clio'; 'cadettes@clio'; 'geert@clio'; 'lisar@clio'; 'solo@clio'; 'tbr@clio'; 'vanthof@hestia'
Subject: Re: ctg and cr metal 5

> Geert sez:
>
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staff place
> > M5 on a 24um by 24um grid so that layouts could be placed in any
orientation.
>
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>
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rotated
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analog blocks
> and since we did not know their orientation, we defaulted to 24 on all
sides
>
>
> On Euterpe, I believe most blocks follow the 24x24 rules, but the
register file
> does not.
>
>
>
Geert

Then I must not have remembered this quite right.
In any event, maybe we could change the new 24um x 24um check into a 4um in the X and 24um
in the Y check. This check is better than no check at all.

Fred.

.

From: Lisa Robinson [lisar@rhodan]
Sent: Tuesday, September 06, 1994 2:56 PM
To: 'Bob Morgan'; 'fur@rhodan'
Cc: 'paulb@mercury'; 'tbr@mercury'

abbott
Subject: microarch manual terminology
In-Reply-To: <199409061632.JAA21522@mercury.microunity.com>
References: <199409061632.JAA21522@mercury.microunity.com>

Bob Morgan wrote (on Tue Sep 6):

Lisa,
What do you think about Scott's idea? Should we
just use "thread"?
Thanks,
Bob

----- Begin Included Message -----

>From fur@quetzalcoatl Fri Sep 2 20:29:34 1994
Date: Fri, 2 Sep 94 20:29:37 -0700
From: fur@quetzalcoatl (Scott Furman)
To: bobm@quetzalcoatl
Subject: microarch manual terminology
Content-Length: 599

I've noticed the use of the word "cylinder" in the microarch document.
Internally, we do indeed use this term, but it will mean nothing to
anyone outside the company. I think that it's confusing to make up
another word when there are already so many equivalent ones available:
processor, PE (processing element), hardware thread, etc.

(The term was coined in a meeting at which some early, disappointing
simulation results were presented. Mouss noted that Euterpe was like
an engine with only one of its cylinders firing.)

I suggest that we denigrate the use of the word "cylinder".

-Scott

----- End Included Message -----

Curtis had stated in a section that was incorporated into the Uarch
document

"We will generally call each hardware thread a cylinder to make it
easier to distinguish from a software thread."

If distinction is necessary then the term cylinder is desirable since
it is already embedded in much of the hardware and software design.

Although cylinder may not be commonly used in this context. It does
not preclude us from using it here provided we adequately explain the

context in which it is being used. (I quite like the term, after all we are engineers!)

Lisa R.

.

From: John Campbell [solo@abderus]
Sent: Tuesday, September 06, 1994 3:26 PM
To: 'Fred Obermeier'
Cc: 'geert@ambiorix'; 'tom@clio'; 'vo@merope'; 'bpw@clio'; 'cadettes@clio'; 'geert@clio'; 'lisar@clio'; 'solo@clio'; 'tbr@clio'; 'vanthof@hestia'
Subject: Re: ctag and cr metal 5

as Fred Obermeier was saying

..
..> Geert sez:

..>
..> >To greatly simplify the assembly process, Geert has had the layout staff place
..> > M5 on a 24um by 24um grid so that layouts could be placed in any orientation.

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..> and since we did not know their orientation, we defaulted to 24 on all sides

..>
..> On Euterpe, I believe most blocks follow the 24x24 rules, but the register file
..> does not.

..> Geert

..
..Then I must not have remembered this quite right.
..In any event, maybe we could change the new 24um x 24um check into
..a 4um in the X and 24um in the Y check. This check is better than
..no check at all.

..
..Fred.

..
vo tells me some cells are placed rotated so this won't work.

regards, EMail solo@microunity.com
solo a.k.a. John Campbell phone 408 734-8100 fax 408 734-8136

From: Mark Hofmann [hopper@cyclops]
Sent: Wednesday, September 07, 1994 11:22 AM
To: 'Fred Obermeier'
Cc: 'fwo@pelagon'; 'geert@cyclops'; 'mudge@cyclops'; 'vo@cyclops'; 'vant@cyclops'
Subject: Re: S.t. and gridness

Fred Obermeier sez:

Mark,
Thanks for the all the leg work.

It looks like your e-mail referred to external pads. External pads don't cause problem if they are on grid. External pads are on grid if they are generated using the baseplate/Makefile.base. Internal pads can be offgrid if the cell is rotated or not appropriate placed.

The problem with orchis is that the cell that contained the pad ring was on grid, but the pad ring was manually placed within testram offset by 200 by 200. 200 was not a mutiple of 24. Effort was taken on testram to put the internal pads back onto the 4 by 24 grid, but the external pad ring was not checked.

In order to kludge orchis, the entire testram was offset back by 200 by 200 within floorplan.ly. This resulted in making the few internal pads offgrid instead of the many outer pad ring. I designed special internal pad cells to correct for the loss of 4um in the vertical direction.

The only work remaining on orchis should be to figure out how to remove the layers that Dave said cause DRC and LVS problems. Something probably has to be drawn in one of the cells on some layer to cut out the layers that Dave reported earlier.

The root problem is that test ram started using the usual flow from baseplate/Makefile.base, but the cell structure was thrown away. But our s.t.'s are built relying on this very cell structure. The padding for both the die and s.t. are derived from the common padlist.lst file. Unfortunately, the original padlist.lst was discarded and had to be rebuilt by hand.

I think an important lesson learned from orchis is that if we want to automatically build an s.t., we should stick to the structure already set up by baseplate/Makefile.base.

Additional constraints need to be placed on the internal pad cells especially if the user wants a SM2 power plane. For orchis, we were lucky that the bias generating pads were far enough apart so that Vpp could be routed on SM2/SM3 to the internal pad.

Fred.

And:

Mark,

I should add that the desire is to try to catch some of the problems before building the S.t. Even a 4um by 24um grid check would help a lot. The final check will be to build an s.t. and run DRC and LVS.
Of course it would be better to check as much before die + s.t. checks.
There are some internal pad to internal pad spacing checks we can perform.

Tom V says:

The randomness in the internal pads come from custom blocks being moved around ,

For example , the gtlb has changed positions and orientation several times on euterpe . A custom block can be mirrored , rotated to make efficient routing an d packing . You can't

always know ahead of time what orientation the block will finally assume .

Sure , we can redo the custom layouts orientation such that all blocks can be placed with a standard orientation today . But we can't guarantee that we won't move things around tomorrow . Or another variant of calliope or euterpe won't want a different floorplan with the same proteus blocks oriented differently .

I say:

Let's do the following: Take the quickest route out of this mess to get Orchis done. we screwed up and did not do Orchis properly- in the future we won't do that, we'll follow our ground rules instead. that will prevent this problem in the future. For now, let's take whatever shortcut we need to get this done. That means not doing a full DRC check if things are too complicated and also doing things manually. Presumably we'll only have to do these things this once. So: let's DRC check for gridness as best we can at the top-level only, let's freeze Orchis and then get the s.t. to work with that frozen design.

Comments?

-hopper
is today, let's fr

From: abbott
Sent: Wednesday, September 07, 1994 3:07 PM
To: 'jsw'
Subject: tasks

Looking at the tasks board, isn't your task "DLWS on terp, tuning real-time part" done?
(Or in remission?)

Also, it looks like the next one "DLWS on terp, API" is quite close.
Care to hazard some dates?

- Curtis

From: Tom Vo [vo@merope]
Sent: Wednesday, September 07, 1994 5:09 PM
To: 'Mark Hofmann'
Cc: 'tvo@cyclops'; 'geert@cyclops'
Subject: Re: S.t. and gridness

Mark Hofmann wrote

>
>Tom Vo sez:
> More confusion still . I thought the problem is with the internal
pads , not
> the ones forming the I/O structures .
>
>Tom-
>
> What's the current layout of the internal pads? Can we standardize on
that?
>

The randomness in the internal pads come from custom blocks being moved around , For
example , the gtlb has changed positions and orientation several times on euterpe . A
custom block can be mirrored , rotated to make efficient routing and packing . You can't
always know ahead of time what orientation the block will finally assume .

Sure , we can redo the custom layouts orientation such that all blocks can be placed with
a standard orientation today . But we can't guarantee that we won't move things around
tomorrow . Or another variant of calliope or euterpe won't want a different floorplan with
the same proteus blocks oriented differently .

tvo

From: Gregg Kellogg [gregg@scylla.microunity.com]
Sent: Wednesday, September 07, 1994 7:31 PM
To: 'lisar'
Subject: Architecture Doc

I'd like to get a copy of the Terpsichore System Architecture Doc. I've a borrowed version dated 4/14/93, perhaps there's something more up-to-date by now. I understand that you're the one to talk to about this.

Gregg Kellogg

--
Gregg Kellogg
gregg@microunity.com

From: Geert Rosseel [geert@rhea]
Sent: Wednesday, September 07, 1994 8:24 PM
To: 'geert@rhea'
Subject: pager log, sender copy

page from geert to geert:
pageme gmake geert_euterpegards start:Sep_07_18:14 end: Sep_07_18:22 exit
1

[Connected]
sending: \015
recv (want ID=/3): ID= -- got it
sending: \033
sending: M
sending: \015
sending: \012
recv (want \012\015\012\015/4): \012\015\012\015 -- got it recv (want Enter the Pager ID,
then RETURN/31): Enter the Pager ID, then RETURN -- got it
sending: 697-3868\015pageme gmake geert_euterpegards start:Sep_07_18:14
end: Sep_07_18:22 exit 1\015
paging geert:
recv (want \015/1): . \012\015 -- got it recv (want Thank You./10): Enter the Message,
then RETURN.
\015\006\015\012\015Thank You. -- got it Page accepted.
sending: exit\012
recv (want \015/1): \012\015 -- got it

.

From: Mark Hofmann [hopper@cyclops]
Sent: Thursday, September 08, 1994 6:57 AM
To: 'Alan Corry'
Cc: 'Mark Semmelmeier'; 'Tim B. Robinson'
Subject: Re: makefile for gards stuff

Alan Corry sez:

I started a gards build from scratch for a new directory UU, and when I say

gmake uugards

it tries to build gards/uu.dff and says it can't, it just gives up. Now if I say:

gmake gards/uu-pass1.pif

it will do this.

```
agc gamorra(79):~/euterpe/verilog/bsrc/uu> gmake uugards
gmake gards/uu.dff
gmake[1]: Entering directory `/N/auspex/root/s33/agc/euterpe/verilog/bsrc/uu'
gmake[1]: *** No rule to make target `gars/uu.dff'. Stop.
gmake[1]: Leaving directory `/N/auspex/root/s33/agc/euterpe/verilog/bsrc/uu'
gmake: *** [uugards] Error 1
```

I've modified the \$(PREIFX)gars target from
\$(MAKE) gards/\$(PREFIX).dff
to
\$(MAKE) gards/\$(PREFIX)-pass1.dff

Things seem to work better now.

-hopper

.

From: Bruce Bateman [stick@kephalos]
Sent: Thursday, September 08, 1994 12:34 PM
To: 'geert@kephalos'; 'tbr@kephalos'; 'mws@kephalos'; 'woody@kephalos'; 'bpw@kephalos'
Subject: .tim, .cap, and .dc files for cache, cahalf, and ctag

.tim, .cap, and .dc files have been created/updated for the cache and tag arrays. The .cap numbers for the cache have been updated to reflect the "reduced capacitance" of the high order read-port address lines whereas the values in the cahalf still contain the old "higher" values. You will recall that this "change" was made just before the euterpe tapeout and thus does not effect the current "snapshot" of calliope.

The .cap values for the ctag now reflect the actual capacitances for the ctag whereas previously we had assumed that they were essentially the same as the cache. For this go-round, I went into the layout and measure actual wire lengths on the ctag.

The values in the .tim file are somewhat "bogus" in that the cache/tag arrays are asynchronous and don't interface directly with the clock tree. Per Mark's suggestion, I have put the following values in:

clk_to_q 1.45ns

This represents the 1.24ns read-port access time (2.9v, 125C, -2 sigma N/P/B models) plus 200ps for the external latches in the SOFA.

setup 1.30ns

This represents the required write-port address setup to the beginning of the write pulse. This time is very conservative, but is used is based on the assumption that the write pulse will be timed to follow the address by two clocks.

These files have all been checked in, but I have not releasebom'ed them please feel free to modify and/or release them as appropriate.

BB

From: Fred Obermeier [fwo@pelagon]
Sent: Thursday, September 08, 1994 4:22 PM
To: 'fwo@pelagon'; 'hopper@cyclops'
Cc: 'geert@cyclops'; 'mudge@cyclops'; 'vant@cyclops'; 'vo@cyclops'
Subject: Re: S.t. and gridness

Hi all,

This M5 stuff looks complicated, but really shouldn't be.

When I first spoke with Haim about implementing such a rule, I said that orchis is a good example of a design that should fail this check while calliope should pass this check. We should ignore these M5 error messages on the internal pads for orchis. The only thing that needs to be completed for orchis s.t. is to remove overlapping mobieclium_noxtors from baseplate/orchistop. The testram should probably have this layer, but nothing else in the orchistop hierarchy should have it. Off hand, I'm not sure what change has to be made to orchis/baseplate/Makefile to subtract this layer from the correct layout cell.

> Vant sez:
> There are mobieclium_noxtors
> placed on top of the wafflization inside the testram area which causes
major
> drc violations and shorts.

Also, Dave reported some shorts problems:

> */W* WARNING ** TEXT : VSSI	1 SHORT DISCARDED
> */W* WARNING ** TEXT : VPP	1 SHORT DISCARDED
> */W* WARNING ** TEXT : VDDE_SENSE	1 SHORT DISCARDED
> */W* WARNING ** TEXT : VDDI	1 SHORT DISCARDED

Later e-mail said that some of these should have gone away. Vssi should be shorted to Vss as per stick, Vpp is routed directly out the Vpp pad on both the die and s.t. SM2/SM3 layers. Vdde_sense is usually shorted to vdde on the internal s.t. SM3 vdde power plane as done for calliope and euterpe. And vddi should be shorted to vdde as per stick.

All in all, the orchis s.t. should be correct, but we just have to make the corresponding changes to get the DRC's and LVS's jobs to pass.

Fred.

From: vant [vanthof@hestia]
Sent: Thursday, September 08, 1994 4:48 PM
To: 'Fred Obermeier'
Cc: 'fwo@pelagon'; 'hopper@cyclops'; 'geert@cyclops'; 'mudge@cyclops'; 'vant@cyclops'; 'vo@cyclops'
Subject: Re: S.t. and gridness

Fred Obermeier writes:

```
>
>> Vant sez:
>> There are mobieclium_noxtors
>> placed on top of the wafflization inside the testram area which
>> causes
major
>> drc violations and shorts.
>
>Also, Dave reported some shorts problems:
>> */W* WARNING ** TEXT : VSSI          1 SHORT DISCARDED
>> */W* WARNING ** TEXT : VPP           1 SHORT DISCARDED
>> */W* WARNING ** TEXT : VDDE_SENSE    1 SHORT DISCARDED
>> */W* WARNING ** TEXT : VDDI          1 SHORT DISCARDED
>
>Later e-mail said that some of these should have gone away. Vssi
>should
be
>shorted to Vss as per stick, Vpp is routed directly out the Vpp pad on
both
>the die and s.t. SM2/SM3 layers. Vdde_sense is usually shorted to vdde
on
>the internal s.t. SM3 vdde power plane as done for calliope and euterpe.
>And Vddi should be shorted to vdde as per stick.
>
>All in all, the orchis s.t. should be correct, but we just have to make
the
>corresponding changes to get the DRC's and LVS's jobs to pass.
>
>Fred.
>
```

The problem with the above shorts is that there is a VSS shorted to VPP and to VDDI and VDDE_SENSE. I believe this might be caused by the fact atoms are placed in areas where thy shouldn't be. Once this is fixed, I'll start up another shorts/lvs run and see if this problem goes away.
My fear is that it won't, but we can hope.

Thanks,
Dave

--
Dave Van't Hof vanthof@microunity.com MicroUnity Systems Engineering,
Inc.
"What rolls down stairs, alone or in pairs, rolls over the neighbor's dog?"

What's great for a snack and fits on your back? It's log, log, log!"
LOG from BLAMMO! (tm) All kids love Log! #include
<std_disclaim.h>

From: Lisa Robinson [lisar@polyhymnia]
Sent: Friday, September 09, 1994 10:27 AM
To: 'craig@polyhymnia'; 'lisar@polyhymnia'
Subject: Registered copy generated

Copy created by: lisar
Copy created at: Fri Sep 9 08:27:14 PDT 1994
Copy number: 273
Copy registered to: Gregg Kellogg
Input file:
/u/craig/documents/Terpsichore/Terpsichore.macps.gz.des
Output file: /u/craig/documents/Terpsichore/Terpsichore.ps
Printed to: rsh plotter lpr -PCraig
Recorded in file: /u/craig/documents/RegistrationLog

[This message generated by /u/craig/bin/macpstops]

From: Mark Hofmann [hopper@cyclops]
Sent: Friday, September 09, 1994 10:47 AM
To: 'Geert Rossee'; 'Brian Lee'
Cc: 'vant@cyclops'
Subject: tim.lib tweak

Hi,

I'm seeing:

Reading Cap/Delay table file
/n/auspex/s32/hopper/chip/euterpe/protelus/leafgen/time/tim.lib

Warning! clk_to_q gate fanin 1 timing value = 0.0 for cell xbhrdf8s at line 135718
Warning! clk_to_q flipflop fanin 1 timing value = 0.0 for cell xbhrdf8s at line 135729
Warning! clk_to_q latch fanin 1 timing value = 0.0 for cell xbhrdf8s at line 135730
Warning! clk_to_q hrflop fanin 1 timing value = 0.0 for cell xbhrdf8s at line 135751
Warning! clk_to_q gate fanin 1 timing value = 0.0 for cell xbhrdf16s at line 135810
Warning! clk_to_q flipflop fanin 1 timing value = 0.0 for cell xbhrdf16s at line 135821
Warning! clk_to_q latch fanin 1 timing value = 0.0 for cell xbhrdf16s at line 135822
Warning! clk_to_q hrflop fanin 1 timing value = 0.0 for cell xbhrdf16s at line 135843
Warning! clk_to_q gate fanin 1 timing value = 0.0 for cell xbhrdf24s at line 135856
Warning! clk_to_q flipflop fanin 1 timing value = 0.0 for cell xbhrdf24s at line 135867
Warning! clk_to_q latch fanin 1 timing value = 0.0 for cell xbhrdf24s at line 135868
Warning! clk_to_q hrflop fanin 1 timing value = 0.0 for cell xbhrdf24s at line 135889
Warning! clk_to_q gate fanin 1 timing value = 0.0 for cell xbhrdf32s at line 135902
Warning! clk_to_q flipflop fanin 1 timing value = 0.0 for cell xbhrdf32s at line 135913
Warning! clk_to_q latch fanin 1 timing value = 0.0 for cell xbhrdf32s at line 135914
Warning! clk_to_q hrflop fanin 1 timing value = 0.0 for cell xbhrdf32s at line 135935

When I run topt. Could you someone please have a look?

-thanks,
hopper

From: Wayne Freitas [wayne@echidna]
Sent: Friday, September 09, 1994 1:24 PM
To: 'hestia@echidna'
Subject: Certification Consultants and UL meeting minutes

FYI,

Over the last several months we have been in the process of evaluating potential vendors to help us in the certification process for Hestia. Below is the list of consultants for the individual areas and a brief status of where we currently stand.

UL/CSA Safety Engineering
 170 Knowles Drive
 Los Gatos, Ca.
 (408) 379-7470
 Contact: Lee Ould Jr., Lee Ould III

See meeting minutes below for current status.

Part 68 (Phone) Clifford Technologies
 962 Coyote St.
 Milpitas, Ca.
 (408) 942-8925
 Contact: Cliff Denchfield

Meeting to be scheduled for end of next week to begin reviewing phone parts list and layout requirements. If your interested in attending meeting please let me know.

EMC	C & C Laboratory 49000 Milmont Drive Fremont, Ca. (510) 440-3838 Contact: Chris Kendall Clark Vitek Sid Johnson	CKC Laboratory 1100 Fulton Place Fremont, Ca. (510) 226-8534 Contact: Kent Chesley Carl Felts
-----	--	---

Open Site Testing 11825 Niles Canyon Rd. Sunol, Ca.	Open Site Testing 1653 Los Viboras Hollister, Ca.
---	---

C & C Labs and CKC Labs both have engineering facilities and consultants available in Fremont for EMC, IEC, and FCC testing. I will arrange to have them come in in a few weeks to provide consultation and review on EMC concerns/requirements pertaining to the main and bandpass PWB's. Please let me know if your interested in attending this meeting.

Meeting minutes from UL review (I have lousy notes so anyone who attended please feel free to add-on anything I missed).

Attendee's: Graham, Tom E., Vijay, John R., Noel, Lee Ould Jr. & III.

Lee Ould gave a presentation of services provided, and what to expect when going through the UL/CSA certification process. Highlighted some of the basic mechanical, thermal and electrical requirements. UL yellow books and a summary of electrical layout rules provide by Safety Engineering.

Explained UL/CSA evolution and major differences between UL 478, UL 1950 with D3 deviations, CSA 950 with D3 deviations and IEC 950. I

have a small handout for anyone interested.

Discussed the issues involving RO's DC-DC convertor. Action Item taken by Noel and Lee Ould to talk with RO to see if RO will do UL 1950 listing for DC- DC convertor.

Discussed UL Listing of Hestia. It was decided to pursue UL 1950 without D3 deviation, and if any problem should arises that would effect Hestia we would fall back to UL 1950 with D3 deviations.

Action Items and agenda for next meeting:

Noel to provide Lee Ould with AC-DC parts listing for review.

Wayne to provide Lee Ould with different certification requirements for review. (done)

Noel & Lee to talk with RO about getting UL 1950 listing for DC-DC convertor. (done)

Safety Engineering to review AC-DC board layout with MUSE personnel for UL/CSA violations. (next meeting) to be schedule.

Safety Engineering to review 1492 Audio/Video requirements against UL 1950 and provide listing of differences. (Hand written handout provide) review next meeting.

Follow-on meeting scheduled to go over the items listed above.

RO Status. RO came by on Tuesday (6th) and indicated that they were willing to go for UL 1950 listing. Lee Ould is going to be working with RO on this.

Wayne

From: Brian Lee [brianl@marathon]
Sent: Friday, September 09, 1994 6:00 PM
To: 'Mark Hofmann'
Cc: 'geert@cyclops'; 'brianl@cyclops'; 'vant@cyclops'
Subject: Re: tim.lib tweak

Mark Hofmann writes:

```
Hi,  
  
I'm seeing:  
Reading Cap/Delay table file  
/n/auspex/s32/hopper/chip/euterpe/teutheus/leafgen/time/tim.lib  
Warning! clk_to_q gate fanin 1 timing value = 0.0 for cell xbhrdf8s at  
line 135718  
Warning! clk_to_q flipflop fanin 1 timing value = 0.0 for cell xbhrdf8s  
at line 135729  
Warning! clk_to_q latch fanin 1 timing value = 0.0 for cell xbhrdf8s at  
line 135730  
Warning! clk_to_q hrflop fanin 1 timing value = 0.0 for cell xbhrdf8s  
at  
line 135751  
Warning! clk_to_q gate fanin 1 timing value = 0.0 for cell xbhrdf16s at  
line 135810  
Warning! clk_to_q flipflop fanin 1 timing value = 0.0 for cell  
xbhrdf16s  
at line 135821  
Warning! clk_to_q latch fanin 1 timing value = 0.0 for cell xbhrdf16s  
at  
line 135822  
Warning! clk_to_q hrflop fanin 1 timing value = 0.0 for cell xbhrdf16s  
at  
line 135843  
Warning! clk_to_q gate fanin 1 timing value = 0.0 for cell xbhrdf24s at  
line 135856  
Warning! clk_to_q flipflop fanin 1 timing value = 0.0 for cell  
xbhrdf24s  
at line 135867  
Warning! clk_to_q latch fanin 1 timing value = 0.0 for cell xbhrdf24s  
at  
line 135868  
Warning! clk_to_q hrflop fanin 1 timing value = 0.0 for cell xbhrdf24s  
at  
line 135889  
Warning! clk_to_q gate fanin 1 timing value = 0.0 for cell xbhrdf32s at  
line 135902  
Warning! clk_to_q flipflop fanin 1 timing value = 0.0 for cell  
xbhrdf32s  
at line 135913  
Warning! clk_to_q latch fanin 1 timing value = 0.0 for cell xbhrdf32s  
at  
line 135914  
Warning! clk_to_q hrflop fanin 1 timing value = 0.0 for cell xbhrdf32s  
at  
line 135935  
  
When I run topt. Could you someone please have a look?  
  
-thanks,  
hopper
```

The zero delays are also present in the original .tim files. I'll try regenerating the

simulation output ...

--

Brian Lee brianl@microunity.com
MicroUnity Systems Engineering (408) 734-8100

From: Geert Rosseel [geert@rhea]
Sent: Friday, September 09, 1994 10:41 PM
To: 'geert@rhea'
Subject: pager log, sender copy

page from geert to geert:

pageme gmake geert_euterpe-iter start:Sep_09_20:23 end: Sep_09_20:39 exit
1

[Connected]

sending: \015

recv (want ID=/3): ID= -- got it

sending: \033

sending: M

sending: \015

sending: \012

recv (want \012\015\012\015/4): \012\015\012\015 -- got it recv (want Enter the Pager ID,
then RETURN/31): Enter the Pager ID, then RETURN -- got it

sending: 697-3868\015pageme gmake geert_euterpe-iter start:Sep_09_20:23

end: Sep_09_20:39 exit 1\015

paging geert:

recv (want \015/1): . \012\015 -- got it recv (want Thank You./10): Enter the Message,
then RETURN.

\015\006\015\012\015Thank You. -- got it Page accepted.

sending: exit\012

recv (want \015/1): \012\015 -- got it

.

From: Geert Rosseel [geert@ambiorix]
Sent: Sunday, September 11, 1994 1:38 PM
To: 'lisar@ambiorix'; 'tbr@ambiorix'
Subject: v2e on euterpe

Hi,

When I run v2e on my current toplevel (cd, cdio, gt, dr, sr, cc, gtlb), it runs fast, however when I include ci (icache) v2e is not able to finish (job size becaomes very large and cpu usage goes to 0) It finally dies with Memory Fault ...

Have you seen thsi ?

Geert

From: vant [vanthof@hestia]
Sent: Sunday, September 11, 1994 4:54 PM
To: 'Geert Rosseel'
Cc: 'vanthof@staypuft'
Subject: Re: Topt core dump

Geert Rosseel writes:

```
>  
>Hi Dave,  
>  
> I get this :  
>  
>/bin/sh: 1431 Memory fault - core dumped  
>gmake[1]: *** [gards/geert_euterpe-pass1.sdl] Error 139  
>  
> The output of the make is in /u/geert/chip/euterpe/bsrc/make.out and  
> all  
the  
>files are still there, including the core file.  
>  
>Geert  
>
```

Sorry for the delay in getting back to you. A comedy of errors have made it difficult and to make it worse, I only have a short amount of time before I leave again. I'll try to track this down.

Thanks,
Dave

--
Dave Van't Hof vanthof@microunity.com MicroUnity Systems Engineering,
Inc.
"What rolls down stairs, alone or in pairs, rolls over the neighbor's dog?"

What's great for a snack and fits on your back? It's log, log, log!"
LOG from BLAMMO! (tm) All kids love Log! #include
<std_disclaim.h>

From: vant [vanthof@hestia]
Sent: Sunday, September 11, 1994 6:16 PM
To: 'Geert Rosseel'
Cc: 'Dave Van't Hof'; 'Mark Hofmann'
Subject: topt installation

Geert,

I found the problem and I've fixed topt. When I ran it on your euterpe, it completed all the way through.

If you run into any problems with this installation, please let me know.

Thanks,
Dawe

--

Dave Van't Hof vanthof@microunity.com MicroUnity Systems Engineering,
Inc.

"What rolls down stairs, alone or in pairs, rolls over the neighbor's dog?"

What's great for a snack and fits on your back? It's log, log, log!"

LOG from BLAMMO! (tm) All kids love Log! #include

<std_disclaim.h>

From: Arya Behzad [arya@aphrodite]
Sent: Monday, September 12, 1994 10:50 AM
To: 'euterpe@aphrodite'
Subject: PLL meeting

From: rich@pegasus (Rich McCauley)
To: graham@pegasus
Subject: euterpe pll design review
Cc: dane@pegasus, ras@pegasus, yves@pegasus, bfox@pegasus, hessam@pegasus, arya@pegasus
Content-Length: 464
X-Lines: 8
Status: RO

There will be a short design review of the vco changes necessary for the 2x frequency output in the sofa clock pll for euterpe. This really shouldn't take long in as the only thing to change is the vcoss. Thus, the items to be presented are simply the freq/gain characteristics of the new vcoss and the resulting loop performance as predicted by linear system equations.

Time: Mon. Sept 12 10am
Place: Analog conference room (crontog2; conf. room next to Graham)

From: Rich McCauley [rich@pegasus]
Sent: Monday, September 12, 1994 11:45 AM
To: 'arya@aphrodite'
Cc: 'euterpe@pegasus'
Subject: Re: PLL meeting

The review is put off a half hour until 10:30 due to a problem with obtaining data output from hspice/gsi.

rich

> From: arya@aphrodite Mon Sep 12 08:50:04 1994
> Date: Mon, 12 Sep 1994 08:49:47 -0700
> From: arya@aphrodite (Arya Behzad)
> To: euterpe@aphrodite
> Subject: PLL meeting
> Content-Length: 694
>
>
> From: rich@pegasus (Rich McCauley)
> To: graham@pegasus
> Subject: euterpe pll design review
> Cc: dane@pegasus, ras@pegasus, yves@pegasus, bfox@pegasus,
hessam@pegasus,
> arya@pegasus
> Content-Length: 464
> X-Lines: 8
> Status: RO
>
> There will be a short design review of the vco changes necessary for
> the
2x
> frequency output in the sofa clock pll for euterpe. This really
shouldn't
> take long in as the only thing to change is the vcoss. Thus, the items
to be
> presented are simply the freq/gain characteristics of the new vcoss and
the
> resulting loop performance as predicted by linear system equations.
>
> Time: Mon. Sept 12 10am
> Place: Analog conference room (crontog2; conf. room next to Graham)
>
>

From: Mark Hofmann [hopper@cyclops]
Sent: Monday, September 12, 1994 12:05 PM
To: 'Geert Rosseel'; 'Tim B. Robinson'; 'Bill Zuravleff'; 'Alan Corry'
Cc: 'vant@cyclops'
Subject: nb status

My latest run of NB has not completed, however the current results do not look promising. At pass3 there are 1810 timing violations. 62 are greater than 300ps, 345 > 200ps, 1046 > 100ps.

The worst offender looks like this:

Warning! Cycle time exceeded by 365.37ps using cycle time of 895.00 for Iteration 4 HARD ERROR 95
Path After Optimization using cycle time of 895.00:
muxenff2_4prbSel/u3/u1 (xbffbdh24s 24S) Oport: q_ad0ph IntDel: 88.10 net: prbSel<3> swg: DH delay: 570.71ps (force) RC delay: 335.53ps lds: 33 pcap: 214.16ff cap: 941.36ff (ext) m1len: 0.00 m2len: 3131.00 m3len: 3403.00
mux4_32prb/u9 (xbmux4dh16s 16S) Iport: SEL_A0PEH<3> Oport: q_and0ph IntDel: 121.70 net: prb_N<9> swg: DH delay: 92.38ps (force) RC delay: 14.95ps lds: 3 pcap: 35.47ff cap: 199.77ff (ext) m1len: 0.00 m2len: 19.00 m3len: 1378.00
muxenff2_5oq/u4/u0 (xbmuxen2dh16s 16S) Iport: D1_AND0PH Oport: q_ad0ph IntDel: 70.10 net: muxenff2_5oq/u4/m swg: DH delay: 9.58ps (force) RC delay: 0.06ps lds: 1 pcap: 7.86ff cap: 21.96ff (ext) m1len: 46.00 m2len: 3.00 m3len: 0.00
muxenff2_5oq/u4/u1 (xbffdh3s 3S) Iport: D0_ADMPH IntDel: 307.80
Time through Path: 1260.37

There is a 3.1mm run on metal2 that's causing problems. But that's not all of it. The long setup time on muxenff2_5oq/u4/u1 (xbffdh3s 3S) is also a contributor.

I don't have a plot of this block but the random logic spans almost 4 clock spars in places (it started out at about 2 clock spars). The pass 3 atom count is: 67784.

If people want to have a look at the job, results will appear in /u/hopper/chip/euterpe/verilog/bsrc/nb/gards

-hopper

From: Sandeep Nijhawan [sandeep@MicroUnity.com]
Sent: Monday, September 12, 1994 12:07 PM
To: 'brendan@MicroUnity.com'; 'fur@MicroUnity.com'; 'abbott@MicroUnity.com';
'gregg@MicroUnity.com'; 'guarino@MicroUnity.com'; 'sandeep@MicroUnity.com'
Subject: ukernel exception model

Last week we had some discussion of what the ukernel exception model should look like. Given below is a user-level description of what I think I am implementing along with a sketch of how the ukernel code would work.

One of the issues we had discussed was whether the exception handler should run in the context of the thread which does the ioctl/syscall or if it should be a separate thread. Making it a separate thread would result in higher overhead and would also require a special syscall which can restart the original thread (which took the exception) at a desired starting point. It would have the advantage of having its own stack which Scott pointed out is convenient for the cache reorganizer tool. In the current model, the exception handler runs on the main thread's stack requiring the cache reorganizer to treat parts of the stack as "hot" and other less frequently used parts as "cold".

Unless we find this to be a major problem, my preference is to stick with the current model but we probably need another meeting to resolve this and perhaps some even more basic questions such as do we need returnable handlers for device exceptions at all (right now there appears to be no reason for having such handlers).

Sandeep

=====

Microkernel Exception and Device Message Model:

Exceptions:

There are two kinds of exception conditions in the ukernel -

- 1) Synchronous exceptions such as addressing and floating point exceptions.
- 2) Asynchronous device related exceptions caused by unusual conditions arising within device drivers such as queue over/underflows, loss of synchronization etc.

The ukernel allows user handlers to be defined for both kinds of exceptions.

Device Messages:

In addition to raising exceptions, device drivers can also cause messages to be sent on certain events such as when a certain number of characters are available to be read or a signal has been acquired etc. User threads can wait for and receive such messages.

I. Synchronous Exceptions:

Handlers for synchronous exceptions are registered using the registerExceptionHandler system call [name preferred over registerReentryPoint] which is

```
registerExceptionHandler(int exceptionMask, void (*handler)(), void *arg, int flags)
```

where arg is simply passed back to the handler at exception time and flags is a bitmask with the following bit values -

HANDLER_RETURNS and HANDLER_SAVES_STATE

The handler is invoked as

```
handler(int exceptionNum, void *arg, void *systemArg)
```

If HANDLER_RETURNS is set but HANDLER_SAVES_STATE is not set, the system saves the full exception state on the current thread's stack and passes a pointer to the saved state as systemArg. The handler can then manipulate the saved state before returning. If HANDLER_SAVES_STATE is set (expected to be done by compiling the handler using the as-yet-unimplemented preserve_regs keyword/pragma) then the system may just save a minimal amount of state necessary to return but nothing more. If flags is zero, which is likely to be the most common case, the handler is expected to never return but to longjmp to some previously determined restart point in the thread. In this case no state is saved.

Returnable exception handlers return to the original thread using the exceptionReturn syscall (since a bdl is no longer available) which is not yet implemented. This syscall would probably look like -
exceptionReturn(exception_context_t *cxt).

Only one synchronous exception handler can be registered per thread using the registerExceptionHandler syscall (to save memory in the ukernel) and subsequent registerExceptionHandler syscalls override previous ones.

Synchronous exceptions occurring in returnable exception handlers themselves can be detected and will be treated as fatal errors (the thread will be killed) but exceptions in non-returnable handlers can cause infinite loops.

The hardware ensures that only one exception occurs at a time and so no masking of exceptions is needed while one is being processed.

II. Device Exceptions:

Certain device-specific conditions cause exceptions to be delivered asynchronously to threads. User handlers for such exceptions are registered using ioctl's. These ioctl's look something like

```
ioctl(fd, dev_ASYNC_EXCEPTION, handler_fn, handler_arg, q_index, ...)
```

(not all devices take a q_index)

The handler is invoked as -

handler (int cause, void *handler_arg, void *system_arg) which is same format as the handler for synch exceptions.

When an asynchronous exception is delivered by a device driver that particular exception is disabled by the driver and the ioctl must be re-issued after the exception has been handled. Other exceptions from the same device may also be disabled on a device-specific basis e.g. when a loss of sync exception is delivered by the TV_IN device, overflow exceptions may be disabled but not vice-versa. In any case, the user must reissue the ioctl after an exception to re-enable all exceptions from that device.

The handler is always invoked in the context of the thread that does the ioctl and can longjmp to restart points within the thread. Device exception handlers are never expected to return (Q: Do we need returnable handlers for device exceptions ?)

Only one device exception handler can be registered per device for the entire task (and since currently there can be just one task owning a device, there can only be one user exception handler per device in the system). Subsequent such ioctl's done by any thread in the task override previous ones done by the same or different thread in that task. Once an ioctl has been issued it may be hazardous (for the task) to reissue another one before an exception has been received (Q: should this be disallowed ?) as there is no provision for maintaining atomicity of user-supplied information set using the ioctl while an exception is being delivered.

III. Device Messages:

Device messages are also enabled by ioctl's such as IR_CMDS_IN_READ_WAIT, TV_IN_TUNE etc. These result in messages sent by the device driver to the user application when the given conditions are satisfied. As an example -

```
ioctl(fd, IR_CMDS_IN_READ_WAIT, size);
```

```
....  
receiveMessage(&thread_id, &msg_code, &msg_arg, 0);
```

would cause the receiveMessage to unblock when size bytes were available to be read from the device queue. thread_id would be set to zero, msg_code and msg_arg would be device specific (zero for this example ? or perhaps msg_code can be IR_CMDS_IN_READ ?)

(Q: What happens if the thread is also being sent some other messages from other threads ? It would be hard to hide the above in a libc 'read' call for example without discarding these)

Microkernel internal :

Devices which can deliver device messages or exceptions are statically assigned a "soft-event" bit in the Euterpe event register. An interrupt handler which runs on an appropriate cylinder (which has no high rate events assigned to it - probably cyl 0) handles these events. This event handler can be "fast" (runs in interrupt mode but is not onchip) or a normal thread (I haven't decided yet). The ukernel keeps an onchip array of uint128s with one member for each soft event. Elements of this array can be set by real-time code as needed for whatever info needs to be passed for that exception. Currently we think that two octlets are enough for such info but we could make arrangements for the second octlet to be a ptr to a device-specific message buffer. Both device exceptions and device messages allow two octlets of info to be delivered directly via (cause, systemArg) and (msgCode, msgArg). A single "action" bit in the first octlet tells the interrupt handler whether a message should be sent or an exception generated for that soft event.

The ukernel also keeps an offchip array with one element for each soft event number. This has information which can be set at ioctl time such as the thread_id which will get the exception, handler_pc, handler_dp and the user-passed handler_arg and the soft-event handler also uses this to send a message or generate an exception.

From: abbott
Sent: Monday, September 12, 1994 1:21 PM
To: 'Kevin Peterson'
Subject: qam receiver state diagrams

Kevin Peterson wrote (on Mon Sep 12):

Where can I find the QAM receiver state diagrams? I want to print out a copy for myself. BTW, I'm handing off the rest of the mpeg audio

It's a frame document in ~abbott/docs/dsp-block-diagram; some pages in the middle.

integration to Brendan and Scott (which is almost done) so that I can start working exclusively on the terp track of the QAM receiver.

Sounds good.

- Curtis

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From: Jay Tomlinson [woody@melpomene]
Sent: Monday, September 12, 1994 3:20 PM
To: 'mws@melpomene'; 'billz@melpomene'
Cc: 'tbr@melpomene'; 'woody@melpomene'
Subject: I-Cache Control

Mark, Bill,

Following is what I think is the bulk of what needs to be done in order to implement I-cache operations. I am willing to bet that I missed something, but in general tried to point at the major function that needs to be added.

Let me know if you think of anything that should be on the list.

thanks,
Jay

I-Cache Operations:

The itag is accessed/checked when the instruction is actually being executed. This means that if ciMiss then the current instruction must be cancelled and ife'ing of that cylinder will be stopped. The nb request to fetch the icache line cannot be initiated by this flow because ife does not have access to its physical address. Therefore, a 'psuedo-branch'(BFetch) flow must be generated by UU in response to the ciMiss. This flow will use the NRMLEX access type which will enable translation, exceptions, and the 1st NB request to occur. This means that the phys address will be created. 3 more NB requests must be generated to complete the cache line. The initial NB request that is generated by LT must set the CACHE bit to 1 and also set the ICACHE/DCACHE bit to 1. These bits will be used by CC to generate the NB request necessary to complete the ICACHE line.

When each requests NB data returns, UU will generate a 'psuedo-op' (SN128WrtI) that load will from NB and stores to the IBUF (an NB request). This job's access type will use an access type that disables exception reporting. UU must also generate a control signal that will force LT to convert the address (cache index?, ifp?) into the appropriate IBUF physical address. NB must guarantee that the store request will be accepted. Otherwise the store data will be lost.

The IBUF write control logic (gt/gtsnake) will generate a signal that indicates IBUF write & pbb<CACHE>==1. This will be used by CC to determine when the last octlet has been written which will trigger the write of the ITAG. This will also signal IFE that the appropriate cylinder can continue execution.

Load/Store conflict detection must be performed to guarantee correct SRAM operation. This will be done adding a comparator in CJ that compares the read and write addresses. The controls from gt/gtsnake will be used to validate the compare result. When a conflict is detected, the IFE will be notified. IFE will ignore the data and re-fetch the line that got the conflict.

Actions:

woody:

1. add a block to generate the ciMiss and perform itag protection checking.
2. add ctioi and new block to euterpe.V
3. add necessary logic to LT to 'generate' IBUF physical address.

4. modify LT, if needed, to perform translation and exception checking/reporting for access type == NRMLEX.
5. modify LT to perform translation and exception checking/no reporting for access type == TRGTEX.
6. modify LT to set nbcin CACHE and ICACHE/IDCACHE bits.
7. modify GTsnake logic to send notification that I-cache write completed. This is sent to CC to trigger the I-cache tag write.
8. Add load/store conflict detection logic to CJ.

billz:

1. modify CC to generate NB requests for I-cache misses.
2. modify CC to write I-cache tag.
3. modify CC to notify IFE that I-cache tag has been written.
4. modify NB to guarantee that IBUF store request will capture an NB entry.

mws:

1. modify IFE to stop fetching (only appropriate cylinder) following a cache miss. Signal from CC will re-enable instruction fetching.
2. modify UU to add BFetch instruction for initiating the NB requests for the I-cache miss.
3. modify UU to add SN128WrtI instruction to receive NB data and send controls to LT to generate an IBUF store NB request.
4. modify UU to support I-fetch tag and GTLB exceptions.
5. modify IFE to re-fetch line when CJ detects a load/store conflict.

From: jt@microunity.com
Sent: Monday, September 12, 1994 7:26 PM
To: 'euterpe@microunity.com'
Subject: FINAL DECISION: Formed Leads for TAB/OLB

>Date: 12 Sep 1994 16:21:36 -0800
>From: "trancy" <trancy@charybdis>
>Subject: FINAL DECISION: Formed Leads for TAB/OLB
>To: "calliope" <calliope@gaea>, "hestia" <hestia@gaea>
>
>The modeling data from Bob (RAS) are not conclusive as comparing the
Formed
>leads vs. Formless leads for TAB/OLB at this moment.
>
>Since we have time constraints for TAB/OLB, it is decided that Formed
leads
>will be used for Calliope and Euterpe during the weekly box group
reviewing
>this morning.
>
>Please call me at X791 if you have any question.
>
>Best regards.
>Trancy.
>
>

John Tang
MicroUnity Systems Engineering, Inc.
255 Caspian Dr. Sunnyvale, CA 94089
(408) 734-8100, (408) 734-8177 fax

Internet: jt@microunity.com

From: tbe@MicroUnity.com
Sent: Monday, September 12, 1994 9:56 PM
To: 'wayne'; 'tbr'; 'noel'; 'woody'; 'graham'; 'bfox'
Cc: 'jt'; 'jr'
Subject: Main PCB criteria

As a followup to Noel's mail regarding UL impact on AC/DC, Wayne initiated a discussion which suggested that the requirement to do HiPot testing on the main pcb could pose an insurmountable problem with respect to cost, yield and reliability, due to either immediate damage to the many expensive components (Caplipoes, Eutepes, SDRAMs, diplexers, etc) from a test failure, or latent damage to same due simply to the test exposure. I also had been looking at the interconnect between the AC-DC and the main pcb, and had determined that the 300 Vdc and return (HazV) had to be separated from the control lines on separate connectors to meet UL spacing requirements in a practical manner.

While we look into this concern further, I am releasing the main pcb criteria as is, so that the PCad designer can get started tomorrow. It seems to be a likely possibility that we will split the main pcb by incorporating the dc-dc into an enlarged ac-dc pcb, and use bus bars, Amp crimp flex, or other power distribution interconnect to bring the low dc voltages to the main. We need to decide this week, I think, and determine the impact on the power and ground planes, etc. I would like to either decide to go this route and issue an "imminent decision" message by Wednesday, or stay the course. In the meantime, the locations of Calliope and Euterpe shouldn't change from the current criteria drawing, and I am checking it in tonight as "mainpcb_criteria" in the "dxf" directory under hestia. Let's discuss at your earliest opportunity.

Regards,

-Tom

Tom Eich tbe@microunity.com
MicroUnity Systems Engineering, Inc.
255 Caspian Dr. Sunnyvale, CA 94089
(408)734-8100, (408)734-8136 fax

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From: Mark Hofmann [hopper@boreas]
Sent: Tuesday, September 13, 1994 12:25 AM
To: 'Geert Rosseel'; 'Tim B. Robinson'; 'Alan Corry'; 'Bill Zuravleff'; 'vant@boreas'
Subject: nb "finished"

with 1250 timing violations; the worst offender is:
Warning! Cycle time exceeded by 899.74ps using cycle time of 926.00 for Iteration 1
pqueuedr/muxff2_5e12/u0 (xbmuxff2df4s 4S) Oport: q_ad0pf IntDel: 134.10 net: pqueuedr/e12<0> swg: DF delay:
1441.24ps RC delay: 9.51ps lds: 2 pcap: 15.51ff cap: 156.81ff(ext) m1len: 0.00 m2len: 311.00 m3len: 856.00
pqueuedr/muxff2_5e12/u0 (xbmuxff2df4s 4S) Iport: D0_AD0PH IntDel: 250.40
Time through Path: 1825.74

which looks kinda funny to me.

Results in ~hopper/chip/euterpe/verilog/bsrc/nb/gards

-thanks,
hopper

.

From: vant [vanthof@hestia]
Sent: Tuesday, September 13, 1994 8:42 AM
To: 'Mark Hofmann'
Cc: 'geert@boreas'; 'tbr@boreas'; 'agc@boreas'; 'billz@boreas'; 'vant@boreas'
Subject: Re: nb "finished"

Mark Hofmann writes:

>
> with 1250 timing violations; the worst offender is:
> Warning! Cycle time exceeded by 899.74ps using cycle time of 926.00 for Iteration 1
> pqueuedr/muxff2_5e12/u0 (xbmuxff2df4s 4S) Oport: q_ad0pf IntDel: 134.10 net: pqueuedr/e12<0> swg: DF
delay: 1441.24ps RC delay: 9.51ps lds: 2 pcap: 15.51ff cap: 156.81ff (ext) m1len: 0.00 m2len: 311.00 m3len:
856.00
> pqueuedr/muxff2_5e12/u0 (xbmuxff2df4s 4S) Iport: D0_AD0PH IntDel: 250.40
> Time through Path: 1825.74
>
> which looks kinda funny to me.
>
> Results in ~hopper/chip/euterpe/verilog/bsrc/nb/gards
>
> -thanks,
> hopper
>

Yes, this is suspicious. Seems like topt didn't power the xbmux up higher
which would have let this path pass.

I'll take a look at it.

Thanks,
Dave

—
Dave Van't Hof vanthof@microunity.com MicroUnity Systems Engineering, Inc.
"What rolls down stairs, alone or in pairs, rolls over the neighbor's dog?
What's great for a snack and fits on your back? It's log, log, log!"
LOG from BLAMMO! (tm) All kids love Log! #include <std_disclaim.h>

From: Mark Hofmann [hopper@cyclops]
Sent: Tuesday, September 13, 1994 9:38 AM
To: 'Geert Rosseel'; 'Tim B. Robinson'; 'Alan Corry'; 'vant@cyclops'
Subject: nb hard errors

The latest version of topt says there are 6 hard errors remaining in NB:

Warning! Cycle time exceeded by 42.85ps using cycle time of 926.00 for
Iteration 1 HARD ERROR 167
ff_pushpqhc1e/u0 (xbffbfdf32s 32S) Oport: q_and0pf
IntDel: 92.10 net: pushpqhc1e swg: DF delay: 315.37ps RC delay: 99.27ps
lds: 18 pcap: 104.56ff cap: 512.16ff (ext) mllen: 0.00 m2len: 2147.00
m3len: 1437.00
pqueuehcl/pqptr/nbpqptrslice8/Uout_1/u0 (xbor4df16s 16S)
Iport: D2_AOPF Oport: q_and0pf IntDel: 121.70 net:
pqueuehcl/pqptr/nbpqptrslice8/out_N_1 swg: DF delay: 208.89ps RC delay:
19.01ps lds: 1 pcap: 5.17ff cap: 196.57ff (ext) mllen: 0.00 m2len:
1540.00 m3len: 374.00
pqueuehcl/pqptr/nbpqptrslice8/Uout/u0 (xborffbf6df32s 32S)
Iport: D1_AOPF IntDel: 230.80
Time through Path: 968.85

Warning! Cycle time exceeded by 67.59ps using cycle time of 926.00 for
Iteration 1 HARD ERROR 178
ff_pushpqhc0d/u0 (xbffbfdf32s 32S) Oport: q_and0pf
IntDel: 92.10 net: pushpqhc0d_N swg: DF delay: 272.67ps RC delay:
82.16ps lds: 16 pcap: 85.63ff cap: 449.73ff (ext) mllen: 0.00 m2len:
1883.00 m3len: 1512.00
pqueuehcl/pqptr/nbpqptrslice2/Uout_3/u0 (xbor4df16s 16S)
Iport: D2_AOPF Oport: q_and0pf IntDel: 121.70 net:
pqueuehcl/pqptr/nbpqptrslice2/out_N_3 swg: DF delay: 276.32ps RC delay:
29.48ps lds: 1 pcap: 5.17ff cap: 257.17ff (ext) mllen: 0.00 m2len:
1676.00 m3len: 598.00
pqueuehcl/pqptr/nbpqptrslice2/Uout/u0 (xborffbf6df32s 32S)
Iport: D3_AOPF IntDel: 230.80
Time through Path: 993.59

Warning! Cycle time exceeded by 8.75ps using cycle time of 926.00 for
Iteration 1 HARD ERROR 219
pqueuehcl/pqptr/nbpqptrslice8/Uout/u0 (xborffbf6df32s 32S)
Oport: q_and0pf IntDel: 92.10 net: pqueuehcl/qfull_N<8> swg: DF
delay: 281.27ps RC delay: 91.51ps lds: 11 pcap: 60.09ff cap:
447.89ff (ext) mllen: 0.00 m2len: 1849.00 m3len: 2029.00
pqueuehcl/pqptr/nbpqptrslice8/Uout_1/u0 (xbor4df16s 16S)
Iport: D0_AOPF Oport: q_and0pf IntDel: 121.70 net:
pqueuehcl/pqptr/nbpqptrslice8/out_N_1 swg: DF delay: 208.89ps RC delay:
19.01ps lds: 1 pcap: 5.17ff cap: 196.57ff (ext) mllen: 0.00 m2len:
1540.00 m3len: 374.00
pqueuehcl/pqptr/nbpqptrslice8/Uout/u0 (xborffbf6df32s 32S)
Iport: D1_AOPF IntDel: 230.80
Time through Path: 934.75

Warning! Cycle time exceeded by 44.92ps using cycle time of 926.00 for
Iteration 1 HARD ERROR 242
pqueuehcl/pqptr/nbpqptrslice1/Uout/u0 (xborffbf6df32s 32S)
Oport: q_and0pf IntDel: 92.10 net: pqueuehcl/qfull_N<1> swg: DF
delay: 250.00ps RC delay: 76.25ps lds: 11 pcap: 54.70ff cap:
408.80ff (ext) mllen: 0.00 m2len: 1595.00 m3len: 1946.00
pqueuehcl/pqptr/nbpqptrslice2/Uout_3/u0 (xbor4df16s 16S)
Iport: D0_AOPF Oport: q_and0pf IntDel: 121.70 net:
pqueuehcl/pqptr/nbpqptrslice2/out_N_3 swg: DF delay: 276.32ps RC delay:
29.48ps lds: 1 pcap: 5.17ff cap: 257.17ff (ext) mllen: 0.00 m2len:
1676.00 m3len: 598.00

pqueuehlc0/ppptr/nbpqptrslice2/Uout/u0 (xborfff6df32s 32S)
Iport: D3_A0FF IntDel: 230.80
Time through Path: 970.92

Warning! Cycle time exceeded by 54.25ps using cycle time of 926.00 for
Iteration 1 HARD ERROR 246

pqueuehlc0/ppptr/ff_r1/u0 (xbffbfdf32s 32S) Oport:
q_ad0pf IntDel: 92.10 net: pqueuehlc0/ppptr/r1 swg: DF delay: 259.34ps RC
delay: 79.86ps lds: 13 pcap: 67.79ff cap: 422.79ff (ext) mllen: 0.00
m2len: 1643.00 m3len: 1907.00
pqueuehlc0/ppptr/nbpqptrslice2/Uout_3/u0 (xbor4df16s 16S)
Iport: D3_A0FF Oport: q_ad0pf IntDel: 121.70 net:
pqueuehlc0/ppptr/nbpqptrslice2/out_N_3 swg: DF delay: 276.32ps RC delay:
29.48ps lds: 1 pcap: 5.17ff cap: 257.17ff (ext) mllen: 0.00 m2len:
1676.00 m3len: 598.00
pqueuehlc0/ppptr/nbpqptrslice2/Uout/u0 (xborfff6df32s 32S)
Iport: D3_A0FF IntDel: 230.80
Time through Path: 980.25

Warning! Cycle time exceeded by 65.88ps using cycle time of 926.00 for
Iteration 1 HARD ERROR 249

pqueuehlc0/nbpqghelper/Ulastb/u0 (xborffb2df32s 32S) Oport:
q_ad0pf IntDel: 92.10 net: pqueuehlc0/lastb swg: DF delay:
270.96ps RC delay: 81.20ps lds: 17 pcap: 86.80ff cap:
447.90ff (ext) mllen: 0.00 m2len: 1828.00 m3len: 1537.00
pqueuehlc0/ppptr/nbpqptrslice2/Uout_3/u0 (xbor4df16s 16S)
Iport: D1_A0FF Oport: q_ad0pf IntDel: 121.70 net:
pqueuehlc0/ppptr/nbpqptrslice2/out_N_3 swg: DF delay: 276.32ps RC delay:
29.48ps lds: 1 pcap: 5.17ff cap: 257.17ff (ext) mllen: 0.00 m2len:
1676.00 m3len: 598.00
pqueuehlc0/ppptr/nbpqptrslice2/Uout/u0 (xborfff6df32s 32S)
Iport: D3_A0FF IntDel: 230.80
Time through Path: 991.88

Total atom count is 44158.

There are 19 DC load violations. The non-xbc01's are:

ERROR! DC Load Underpowered net.
pbben (PBBEN) port: q_ad0ph Lds: 32 Ld Cur: 70.80 OldDr Cur:
59.6
6 PrevDrSz: 24 NewDr Cur: 59.66 CalcDrvSz: 29 NewDrvSz:
24
WireDel: 161.60 xborffb4dh24s (orff4_pbben/u0)

ERROR! DC Load Underpowered net.
cb0a (CB0A) port: q_ad0ph Lds: 32 Ld Cur: 68.95 OldDr Cur: 59.75
PrevDrSz: 24 NewDr Cur: 59.75 CalcDrvSz: 28 NewDrvSz: 24
WireDel:
153.79 xbfdfh24s (ff_1cb0a/u0)

ERROR! DC Load Underpowered net.
cb3a (CB3A) port: q_ad0ph Lds: 32 Ld Cur: 68.95 OldDr Cur: 59.66
PrevDrSz: 24 NewDr Cur: 59.66 CalcDrvSz: 28 NewDrvSz: 24
WireDel:
177.87 xbfdfh24s (ff_1cb3a/u0)

ERROR! DC Load Underpowered net.
cb2a (CB2A) port: q_ad0ph Lds: 32 Ld Cur: 68.95 OldDr Cur: 59.75
PrevDrSz: 24 NewDr Cur: 59.75 CalcDrvSz: 28 NewDrvSz: 24
WireDel:
166.12 xbfdfh24s (ff_1cb2a/u0)

ERROR! DC Load Underpowered net.
cb1a (CB1A) port: q_ad0ph Lds: 32 Ld Cur: 68.95 OldDr Cur: 59.66
PrevDrSz: 24 NewDr Cur: 59.66 CalcDrvSz: 28 NewDrvSz: 24
WireDel:

168.88 xbffbdh24s (ff_lcb1a/u0)

+ several:

ERROR! DC Load Underpowered net.

dbuf/vref_1ph (DBUFVREF_1PH) port: vref_1ph Lds: 1024 Ld

Cur:

1707.00 OldDr Cur: 1619.80 PrevDrSz: 16 NewDr Cur: 1619.80

CalcDrvS

z: 17 NewDrvSz: 16 (forced) WireDel: 3520.55 eawwlvref16s2x4a

(dbuf/w

wlvref0)

Full results in ~hopper/chip/euterpe/verilog/bsrc/nb/gards

-hopper

.

From: tbr
Sent: Tuesday, September 13, 1994 1:07 PM
To: 'Mark Hofmann'
Cc: 'Alan Corry'; 'Mark Semmelmeier'
Subject: Re: makefile for gards stuff
Follow Up Flag: Follow up
Flag Status: Red

Mark Hofmann wrote (on Thu Sep 8):

Alan Corry sez:

I started a gards build from scratch for a new directory UU, and when I say

gmake uugards

it tries to build gards/uu.dff and says it can't, it just gives up. Now if I say:

gmake gards/uu-pass1.pif

it will do this.

agc gamorra(79):~/euterpe/verilog/bsrc/uu> gmake uugards

gmake gards/uu.dff

gmake[1]: Entering directory '/N/auspex/root/s33/agc/euterpe/verilog/bsrc/uu'

gmake[1]: *** No rule to make target 'gars/uu.dff'. Stop.

gmake[1]: Leaving directory '/N/auspex/root/s33/agc/euterpe/verilog/bsrc/uu'

gmake: *** [uugards] Error 1

I've modified the \$(PREIFX)gars target from

\$(MAKE) gards/\$(PREFIX).dff

to

\$(MAKE) gards/\$(PREFIX)-pass1.dff

Things seem to work better now.

That's probably an obsolete target. All you should nee to do in the local Makfile is make the .v2e file and everything else should come from Makefile.share.

Tim

From: Tim B. Robinson [tbr@aphrodite]
Sent: Tuesday, September 13, 1994 1:28 PM
To: 'Geert Rosseel'
Cc: 'lisar@ambiorix'
Subject: v2e on euterpe

Geert Rosseel wrote (on Sun Sep 11):

Hi ,

When I run v2e on my current toplevel (cd, cdio, gt, dr, sr, cc, gtlb), it runs fast, however when I include ci (icache) v2e is not able to finish (job size becaomes very large and cpu usage goes to 0) It finally dies with Memory Fault ...

Have you seen thsi ?

Your INCLUDE list needs updating to reference the behavioral version.
This is also true for cr, tags and gtlb. See the other exampler in the Makefile

Tim

From: Geert Rosseel [geert@rhea]
Sent: Tuesday, September 13, 1994 4:53 PM
To: 'geert@rhea'
Subject: pager log message

page from geert to geert:
pageme gmake geert_euterpegards start:Sep_13_11:57 end: Sep_13_14:52 exit
1

```
[Connected]
sending: \015
recv (want ID=/3): ID= -- got it
sending: \033
sending: M
sending: \015
sending: \012
recv (want \012\015\012\015/4): \012\015\012\015 -- got it
recv (want Enter the Pager ID, then RETURN/31): Enter the Pager ID, then RETURN -- got it
sending: 697-3868\015pageme gmake geert_euterpegards start:Sep_13_11:57
end: Sep_13_14:52 exit 1\015
paging geert:
recv (want \015/1): . \012\015 -- got it
recv (want Thank You./10): Enter the Message, then RETURN.
\015\006\015\012\015Thank You. -- got it
Page accepted.
sending: exit\012
recv (want \015/1): \012\015 -- got it
```

.

From: tbr
Sent: Tuesday, September 13, 1994 9:40 PM
To: 'lisar'
Subject: forwarded message from tbr
Follow Up Flag: Follow up
Flag Status: Red

----- Start of forwarded message -----
In-Reply-To: <199409131755.KAA13394@merope.microunity.com>
References: <199409131755.KAA13394@merope.microunity.com>
To: vo@merope (Tom Vo)
Cc: bobm@merope (Bob Morgan)
Subject: changes to knob assignment

Tom Vo wrote (on Tue Sep 13):

I'd like to reassign some the knobs on euterpe to fix
a routing problem .

The new assignment would read :

octlet 29 , bits 63..56 , reserved .
octlet 28 , bits 63..56 , stack sensor iobyte1 generic bias .
octlet 28 , bits 23..16 , iobyte1 quadrature .

Octlet 29 , bits 63..56 used to be iobyte1 quadrature . As it
turned out , this knob was rendered unroutable by the cr block .

No problem, just do it.

Tim

----- End of forwarded message -----

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From: tbr
Sent: Tuesday, September 13, 1994 11:42 PM
To: 'vanthof'
Subject: bad edif
Follow Up Flag: Follow up
Flag Status: Red

I just got an exit code of 4 from topt, which I have not seen before.
The log file looked OK up to the point where it quit. Any ideas what
would cause this?

Atoms: count atom bjt isrc pld clock
BJT Totals: 1755 15010 27645 19589 22644 12701

Generating instance drive strength file tbr2_euterpe-pass1.strength
Disgorging sdl file gards/tbr2_euterpe-pass1.sdl
Writing sdl structure: tbr2_95_euterpe_46_edif
Memory usage: 34.665MB
Exit code: 4 (Bad Edif)
make[1]: *** [gards/tbr2_euterpe-pass1.sdl] Error 4
rm tbr2_euterpe.v
make[1]: Leaving directory `/N/auspex/root/s15/tbr/euterpe/verilog/bsrc'
make: *** [tbr2_euterpegards] Error 1

.

From: vant [vanthof@hestia]
Sent: Wednesday, September 14, 1994 12:14 AM
To: 'Tim B. Robinson'
Cc: 'vanthof@aphrodite'
Subject: Re: bad edif

Tim B. Robinson writes:

>
>
>
>I just got an exit code of 4 from topt, which I have not seen before.
>The log file looked OK up to the point where it quit. Any ideas what
>would cause this?
>
>
>Atoms: count atom bjt isrc pld clock
> BJT Totals: 1755 15010 27645 19589 22644 12701
>
> Generating instance drive strength file tbr2_euterpe-pass1.strength
> Disgorging sdl file gards/tbr2_euterpe-pass1.sdl
> Writing sdl structure: tbr2_95_euterpe_46_edif
>Memory usage: 34.665MB
>Exit code: 4 (Bad Edif)
>make[1]: *** [gards/tbr2_euterpe-pass1.sdl] Error 4
>rm tbr2_euterpe.v
>make[1]: Leaving directory `/N/auspex/root/s15/tbr/euterpe/verilog/bsrc'
>make: *** [tbr2_euterpegards] Error 1
>

exit code 4 is caused by something wrong with the input edif netlist or some associated file which attempts to deal with the edif. The problem you are having is the latter. The tbr2_euterpe-pass1.topt.log has several errors dealing with the pincap file and the pin names for CR. Here's an example from the topt.log file:

Error! Attempting to attach cap data to Pin SADD0_AD0PEH<0> but pin does not exist on cr

When I look at the edif netlist, the CR pin name is SADD0_A0PEH<0> which is missing the 'D' in the qualifier yet the cap.lib file has a pin name with the 'D' in the qualifier.

Somewhere along the line, the pin names were changed but not updated in both places.

If you don't think this should be a 'high priority' exit status, then I can change the topt behaviour. Also, the topt.log file uses 'Error' instead of 'ERROR' for this particular case. Do you wish this to be changed as well?

Hope this helps.

Thanks,

Dave

--

Dave Van't Hof vanthof@microunity.com MicroUnity Systems Engineering, Inc.

"What rolls down stairs, alone or in pairs, rolls over the neighbor's dog?

What's great for a snack and fits on your back? It's log, log, log!"

LOG from BLAMMO! (tm) All kids love Log! #include <std_disclaim.h>

From: tbr
Sent: Wednesday, September 14, 1994 12:34 AM
To: 'vant'
Cc: 'vanthof@aphrodite'
Subject: Re: bad edif
Follow Up Flag: Follow up
Flag Status: Red

vant wrote (on Tue Sep 13):

Tim B. Robinson writes:
>
>
>I just got an exit code of 4 from topt, which I have not seen before.
>The log file looked OK up to the point where it quit. Any ideas what
>would cause this?
>
>
>Atoms: count atom bjt isrc pld clock
> BJT Totals: 1755 15010 27645 19589 22644 12701
>
> Generating instance drive strength file tbr2_euterpe-pass1.strength
> Disgorging sdl file gards/tbr2_euterpe-pass1.sdl
> Writing sdl structure: tbr2_95_euterpe_46_edif
>Memory usage: 34.665MB
>Exit code: 4 (Bad Edif)
>make[1]: *** [gards/tbr2_euterpe-pass1.sdl] Error 4
>rm tbr2_euterpe.v
>make[1]: Leaving directory `/N/auspex/root/s15/tbr/euterpe/verilog/bsrc'
>make: *** [tbr2_euterpegards] Error 1
>

exit code 4 is caused by something wrong with the input edif netlist or some associated file which attempts to deal with the edif. The problem you are having is the latter. The tbr2_euterpe-pass1.topt.log has several errors dealing with the pincap file and the pin names for CR. Here's an example from the topt.log file:

Error! Attempting to attach cap data to Pin SADD0_A0PEH<0> but pin does not exist on cr

When I look at the edif netlist, the CR pin name is SADD0_A0PEH<0> which is missing the 'D' in the qualifier yet the cap.lib file has a pin name with the 'D' in the qualifier.

It's possible we have a discrepancy between the behavioral model for cr and the real one. I'll check that. If not then the problem is in the cap.lib entry and we should fix that.

Somewhere along the line, the pin names were changed but not updated in both places.

If you don't think this should be a 'high priority' exit status, then I can change the topt behaviour. Also, the topt.log file uses 'Error' instead

of 'ERROR' for this particular case. Do you wish this to be changed as well?

What would the effect be on the generated .sdl file if you had allowed this one through.

Hope this helps.

Yes, thanks.

Tim

From: abbott
Sent: Wednesday, September 14, 1994 12:51 PM
To: 'bobm'
Cc: 'lisar'
Subject: Euterpe MicroArchitecture Document

Lisa - I'd definitely like a paper copy.

Bob - This is very exciting. It looks like a lot of progress has been made. Here are some comments gleaned on a quick pass through the document.

Intro:

I've been trying to deemphasize the term "cylinder". I think it confuses outsiders and isn't truly necessary. I'd prefer it didn't appear in this document. Just say "hardware thread" where it matters.

might mention SRAM cache size is configured from cerberus

under "cache", you say no-alloc loads have variable latency but not that they're non-blocking. I haven't found that anywhere else yet -- it probably deserves a mention here.

Memory Hierarchy:

p 2. the byte-at-a-time control paragraph. That involves the detail exceptions, right? I thought they weren't implemented. In which case, this paragraph should either be deleted or turned into a "difference from TSA" statement.

p 2. the last paragraph is a bit disconnected. Eg the sentence about address widths. that's in TSA and already stated elsewhere.

also the "2-bit field in access info" -- I assume you mean in gtlb or ltlb, where the field is compared against the current privilege level, so that sentence is wrong, or at best, confusing.

p 5. Hermes. No, the 2 hermes channels aren't used one for in and one for out, they're both bidirectional.

p 5. DRAM. cerb config probably applies to more than size?

p 5. ROM. typo in 1st line. incomplete?

p 6, para 3. suggest replace "indiv 64-bit field" with "octlet".

p 6. I assume gtlb addressing is spread out so we can put each entry on a separate page? This is probably worth a mention.

p 7. footnote a. suggest text should be more like "in Euterpe, these fields are always zero; writing a non-zero value to them has no effect".

p 8. The LVA->PA translation formulae should mention differences (for LTLB) if priv level >= 2. Also, it should say what happens in the gtlb if multiple hits.

p 11. NB enqueueing. note that there's a discussion going on about generalizing the mechanism you describe to something involving masks.
stay tuned!

p 12. The NB entry that you document is not programmer visible, right?
this should be mentioned!

Opcodes:

In a public version of this document, I assume we'll want to combine the first 3 colors, so we're only making 2 distinctions -- in or out.

Reset, Events, Cerberus:

I haven't had time to go through these in detail -- they look good at first glance.

- Curtis

From: abbot
Sent: Wednesday, September 14, 1994 6:37 PM
To: 'bobm'
Subject: more comments on euterpe uArch draft

Events and Threads:

p 1. I'm confused about why the chapter's called that. It corresponds to a section in TSA, is that it? But it's not really about threads.

p 1. the second paragraph is confused. There are no more event threads. The Euterpe processor provides resources for 5 threads.
Is TSA to be modified to talk about interrupts or does that need to be deocumented as a difference?

p 2. more about offsets. I asked about the gtlb entry offsets by 0x20 this morning; I now realize it's because a tble entry is 4 octlets, so there are no gaps. So cancel that question. On the other hand, the event regs are octlets, so why hexlet separation?

p 2. interrupt misspelled twice. also, the mask register stuff could be clearer. the notion of "covering" a bit isn't defined, and probably isn't the best word. I think this part could profitably be lengthened.

Lots more stuff about interrupts should be defined. For example, event (a.k.a. interrupt) mode. An explanation of how interrupt handling occurs would be helpful. Gmo or Sandeep should be able to help.

Reset:

p 1. Wrong. No event thread. All threads start from same vector, use thread number bit to decide what to do.

p 3. last paragraph. You mention the registers might be largely right; you don't mention the SRAM. Tim has explained that this is very likely to survive, except maybe location 0. I'd ask someone in HW for a fuller explanation -- this is useful information I think and should be expanded.

Cerberus:

p 1. paragraph 3. a section name might be more stable than a page ref to TSA, unless you've got the documents linked :-)

p 2. in the figure, I'd either duplicate the TSA table saying what each field means or refer explicitly to it.

p 3-x I'd like if it were more explicit about diffs from TSA. Or at least consider that. Maybe only a comment about how the arch codes, etc., correspond to Terpsichore.

p 8. I see a lot of DRAM config stuff here -- this is a place you could point in the DRAM intro place I mentioned in this morning's message.

- Curtis

From: vant [vanthof@hestia]
Sent: Wednesday, September 14, 1994 7:25 PM
To: 'Orlando Hernando'; 'Mike Wageman'
Cc: 'Dave Van't Hof'; 'Geert Rosseel'; 'Mark Hofmann'; 'Tom Vo'
Subject: euterpe lower drc's done

Hi guys.

The first pass at lower drc's finished for euterpe. They are:

/u/vanthof/compass/mobi/euterpe/euterpe_lower.err

It's about 176KB which isn't too bad. This version does have some known problems with atoms missing at the edges of some blocks.

Thanks,

Dave

--

Dave Van't Hof vanthof@microunity.com MicroUnity Systems Engineering,
Inc.

"What rolls down stairs, alone or in pairs, rolls over the neighbor's dog?"

What's great for a snack and fits on your back? It's log, log, log!"

LOG from BLAMMO! (tm) All kids love Log! #include

<std_disclaim.h>

From: Curtis Abbott [abbott@tallis]
Sent: Wednesday, September 14, 1994 8:37 PM
To: 'geert@tallis'
Subject: this just in from the MIT cabal

Henry sent this to me and to Mouss. This one is definitely outside my range of interests.

- Curtis

From: younis@ai.mit.edu (Saed Younis)
Subject: Leads..
To: mike@media-lab.media.mit.edu
Date: Wed, 14 Sep 94 14:59:03 EDT
X-Mailer: ELM [version 2.3 PL0]

Hello,
I just got my Phd in EECS from the AI lab and I'm looking for employment.
I'm trying to get employment leads to send resume's to and I was told by Kleantis that you are the person to talk to. In specific I was wondering if you had information about Micro Unity. Below, I'm including a text copy

of my resume to give an idea about what I've been doing.

I thank you for your time.

Saed Younis

XX

Saed G. Younis
Massachusetts Institute of Technology
Artificial Intelligence Laboratory, Rm. 705
545 Technology Square, Cambridge, MA 02139
(617) 253-8829 Office, (617) 742-4092 Home
younis@ai.mit.edu

PROFESSIONAL
INTEREST: Multi-disciplinary development of Computer and
----- Telecommunications Hardware.

EDUCATION:

September, 1994 Massachusetts Institute of Technology, PhD in Electrical
Engineering and Computer Science with a minor in
semiconductor device physics. Emphasis is on low power
circuits and special purpose computer architecture.
January, 1989 Massachusetts Institute of Technology, SM in Electrical
Engineering and Computer Science.
June, 1986 Massachusetts Institute of Technology, BS in Electrical
Engineering.

EXPERIENCE:

August 1992- Co-inventor of Charge Recovery Logic (CRL) and Split-Level
Present Charge Recovery Logic (SCRL). CRL and SCRL are new CMOS
logic families with a power dissipation that falls with the
square of the operating frequency, unlike the linear drop of
conventional CMOS circuits. SCRL, which is an improvement
on the original CRL, uses 2 times as many devices as
conventional CMOS, needs two external inductors for an entire
chip, and requires no special fabrication process to achieve

orders of magnitude in power savings over conventional CMOS. SCRL is ideally suited for portable information systems. First silicon of an 8x8 multiplier in SCRL (SCRL-1) correctly demonstrated SCRL operation.

January-
August 1992

Designed and implemented the inner shell of a software package for the simulation of hydrodynamic phenomena for a

new multi-speed lattice gas algorithm utilizing the face-centered-hyper-cubic (FCHC) lattice. The platform supported varying particle numbers, inclusion of future instrumentation, run-time programmable software block insertion, completely variable 3D geometry handling and multigridding. The code also had provisions for multi-tasking.

June-
1
August 1991

Designed the microcode controller for Cyclops, a proposed

Teraflop SIMD IBM supercomputer. Work was performed at IBM T. J. Watson research center.

June 1986-
January 1991
to

Designed and implemented a 256-bit number theoretic computer called 'Little Fermat'. The computer was built

efficiently solve problems requiring operations on large numbers (1.2 million decimal digits long). The computer had hardware support for arithmetic modulo $(2^{256})+1$ with residue reduction built in. Additional features included hardware support for conditional-free nested looping and nested subroutine calls. The project was started at IBM T. J. Watson research center and was completed at MIT.

I was responsible for both the hardware and the software sides of the project. Little Fermat is extremely efficient in running Fermat Number Transforms that can perform convolution on data sequences with large dynamic range and no roundoff

error. Little Fermat contains 6600 chips connected by 84,000 wire-wrapped wires. Little Fermat was reported in the October 6th 1990 issue of Science News.

July-
September 1993

Designed the interprocessor high speed network links for a massively parallel computer at Exa Corporation (Cambridge MA).

June-
channel
September 1984

Worked on the early design of the PCCA (IBM PC to 370 adapter) communications board. The initial design was to enable a PC to directly talk to the channel at 3.3 MBytes/s. Later versions of the PCCA have become a successful IBM product and a standard for PC to Host communications. Work was done at IBM T.J. Watson research center.

June 1985-
June 1986
to

Designed and built the clock distribution system for the Multiprocessor Emulation Facility at MIT. The system was

distribute a clock to 64 physically distant processors.

The

completed system could semi-automatically recalibrate itself and could detect open circuits and shorts. The system maintained electrical isolation between the clock tree and

the processors to aid in fault isolation.

September-
December 1989
airplanes.

Designed the layout of a custom VLSI chip to facilitate embedded microcomputer control of radio controlled

Cumulative

Extensive working knowledge of FORTRAN, C, C++, SCHEME, PASCAL, REXX, and YOUNIS code (YOUNIS runs on Little Fermat). Extensive working knowledge in system and VLSI design and debugging tools (BLE, Cadence). Experienced in ALU design for modular arithmetic and the design of general purpose programmable microcode controllers. Experienced in special

purpose hardware, optimized for the solution of large problems. Experienced in high speed inter-system synchronization and communication. Expert in asymptotically zero-energy CMOS (CRL, SCRL). }

Honors:

June 1986

First Prize in the Ernest Guillemin award for the best undergraduate thesis in Electrical Engineering at MIT.

PUBLICATIONS:

``A Design of a General Purpose Number-Theoretic Computer'', in Proceedings of the third International Conference on Supercomputing, Boston, 1988.

``Practical Implementation of Charge Recovering Asymptotically Zero Power CMOS'', in Proceedings of Symposium on Integrated Systems, MIT Press, March 1993.

``Asymptotically Zero Energy Split-Level Charge Recovery Logic'', in Proceedings of 1994 International Workshop on Low Power Design, Napa, April 1994.

INTERESTS:

Is always interested in gaining new experiences pertaining to the performance of skills and achieving understanding about the workings of things and processes. Skills included SCUBA diving (certified), hang gliding, soaring, white-water rafting, sculling, sailing, and sky diving. Skills include photography and processing, radio controlled model construction, electronics, weather satellite tracking and picture decoding (NOAA 9-12), and an insatiable interest in examining new devices closely... (apart).

.

From: tbr
Sent: Wednesday, September 14, 1994 10:18 PM
To: 'Geert Rosseel'
Subject: euterpe/verilog/bsrc Makefile.tst
Follow Up Flag: Follow up
Flag Status: Red

Geert Rosseel wrote (on Wed Sep 14):

Update of /u/chip/chip-archive/euterpe/verilog/bsrc
In directory ghidra:/s3/geert/euterpe/verilog/bsrc

Modified Files:
Makefile.tst
Log Message:

fixed bug :

don't prune list : get \$\$2 not \$\$1 from strength files

Oops! sorry about that. I have still not been able to get rg to run to be able to test it. I think there is still a topt problem. I'm seeing cases where it's leaving timing vioations where things could be powered up. I'm still investigating. . .

Tim

From: Tim B. Robinson [tbr@aphrodite]
Sent: Wednesday, September 14, 1994 10:18 PM
To: 'Geert Rosseel'
Subject: euterpe/verilog/bsrc Makefile.tst

Geert Rosseel wrote (on Wed Sep 14):

Update of /u/chip/chip-archive/euterpe/verilog/bsrc
In directory ghidra:/s3/geert/euterpe/verilog/bsrc

Modified Files:
 Makefile.tst
Log Message:

fixed bug :

don't prune list : get \$\$2 not \$\$1 from strength files

Oops! sorry about that. I have still not been able to get rg to run to be able to test it. I think there is still a topt problem. I'm seeing cases where it's leaving timing vicoations where things could be powered up. I'm still investigating. . .

Tim

From: Geert Rosseel [geert@rhea]
Sent: Wednesday, September 14, 1994 10:47 PM
To: 'geert@rhea'
Subject: pager log, sender copy

page from geert to geert:

pageme gmake geert_euterpegards start:Sep_14_20:15 end: Sep_14_20:44 exit

1

.

From: tbr
Sent: Wednesday, September 14, 1994 11:42 PM
To: 'geert'; 'vo'; 'dickson'; 'agc'
Subject: euterpe atom count
Follow Up Flag: Follow up
Flag Status: Red

I got a top pass1 atom count for the whole of euterpe at a cycle tie of 926. It reports 10038 failing timing paths and an atom count of 360634.

The baseplate currently has 481389 atoms so this would result in a utilization of 75%. If these numbers can be believed, it sure looks like we ought to be able to build it.

Tim

From: Tim B. Robinson [tbr@aphrodite]
Sent: Wednesday, September 14, 1994 11:42 PM
To: 'geert@aphrodite'; 'vo@aphrodite'; 'dickson@aphrodite'; 'agc@aphrodite'
Subject: euterpe atom count

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Tim

From: Tim B. Robinson [tbr@aphrodite]
Sent: Wednesday, September 14, 1994 11:42 PM
To: 'geert@aphrodite'; 'vo@aphrodite'; 'dickson@aphrodite'; 'agc@aphrodite'
Subject: euterpe atom count

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The baseplate currently has 481389 atoms so this would result in a utilization of 75%. If these numbers can be believed, it sure looks like we ought to be able to build it.

Tim

by aphrodite.microunity.com (8.6.4/muse-sw.2)
id JAA00719; Thu, 15 Sep 1994 09:02:22 -0700
Received: from localhost by ambiorix.microunity.com (8.6.4/muse-sw.2)
id JAA00244; Thu, 15 Sep 1994 09:02:26 -0700
Date: Thu, 15 Sep 1994 09:02:26 -0700
From: geert@ambiorix (Geert Rosseel)
Message-Id: <199409151602.JAA00244@ambiorix.microunity.com>
To: geert@aphrodite, tbr@aphrodite
Subject: Re: sc timing data
Status: O

Hi,

This should have fixed it .. I'll have to talk to Dave now ..

Geert

.

From: tbr
Sent: Thursday, September 15, 1994 12:01 AM
To: 'geert'; 'tom'; 'dickson'; 'bill'
Subject: scgcbfr0, scgcdr1
Follow Up Flag: Follow up
Flag Status: Red

What is the status of these two cells? We have one instance of clcgdr1 and 2 of clcgcbfr0 in euterpe and these were supposed to get replaced by sc cells. We seem to have a verilog model and a schematic for scgcbfr0, but not for scgcdr1.

I think it is the case that we can eliminate the clcgdr1 altogether without replacing it by the sc variety, because it is only used in series with a clcgcbfr0 to make a 0p to 2p clock driver and we now have a "scgcdr" which seems to do that in a single cell.

If everyone agrees this substitution is acceptable, rich can you change ck_fgcn to use just a single scgcdr instead of this combination please?

The other clcgcbfr0 is in cp.V and it looks to me like this should be showing as a csyn error because the 1p output of this is being used as a clock to iosynch, which ought to be a 2p clock. That being the case it looks like this one should be a scgcdr also. Rich can you check this please?

Tim

From: Tim B. Robinson [tbr@aphrodite]
Sent: Thursday, September 15, 1994 12:01 AM
To: 'geert@aphrodite'; 'tom@aphrodite'; 'dickson@aphrodite'; 'bill@aphrodite'
Subject: sccgbfr0, sccgdr1

What is the status of these two cells? We have one instance of clcgdr1 and 2 of clcgbfr0 in euterpe and these were supposed to get replaced by sc cells. We seem to have a verilog model and a schematic for sccgbfr0, but not for sccgdr1.

I think it is the case that we can eliminate the clcgdr1 altogether without replacing it by the sc variety, because it is only used in series with a clcgbfr0 to make a 0p to 2p clock driver and we now have a "sccgdr" which seems to do that in a single cell.

If everyone agrees this substitution is acceptable, rich can you change ck_fgen to use just a single sccgdr instead of this combination please?

The other clcgbfr0 is in cp.V and it looks to me like this should be showing as a csyn error because the 1p output of this is being used as a clock to iosynch, which ought to be a 2p clock. That being the case it looks like this one should be a sccgdr also. Rich can you check this please?

Tim

.

From: tbr
Sent: Thursday, September 15, 1994 1:05 AM
To: 'geert'
Subject: sc timing data
Follow Up Flag: Follow up
Flag Status: Red

I saw your check in of fixes to the sc1p etc timing data format.
However, I am still seeing:

Warning! sc2p8 flipflop fanin 17 timing value = 0.0 for cell /n/auspex/s15/tbr/euterpe/proteus/custom/time/tim.lib at line 83
WhatDelayType: Warning! Unknown delay type sc2p8 at line 83 for ce
ll /n/auspex/s15/tbr/euterpe/proteus/custom/time/tim.lib

Warning! sc2p3 gate fanin 17 timing value = 0.0 for cell /n/auspex/s15/tbr/eutepe/proteus/custom/time/tim.lib at line 79
WhatDelayType: Warning! Unknown delay type sc2p3 at line 79 for ce
ll /n/auspex/s15/tbr/euterpe/proteus/custom/time/tim.lib

Warning! sc1p8 latchlatch fanin 17 timing value = 0.0 for cell /n/auspex/s15/tb/euterpe/proteus/custom/time/tim.lib at line 75
WhatDelayType: Warning! Unknown delay type sc1p8 at line 75 for ce
ll /n/auspex/s15/tbr/euterpe/proteus/custom/time/tim.lib

Warning! sc1p3 hrflop fanin 16 timing value = 0.0 for cell /n/auspex/s15/tbr/euerpe/proteus/custom/time/tim.lib at line 71
WhatDelayType: Warning! Unknown delay type sc1p3 at line 71 for ce
ll /n/auspex/s15/tbr/euterpe/proteus/custom/time/tim.lib

Tim

From: Tim B. Robinson [tbr@aphrodite]
Sent: Thursday, September 15, 1994 1:05 AM
To: 'geert@aphrodite'
Subject: sc timing data

I saw your check in of fixes to the sc1p etc timing data format.
However, I am still seeing:

```
Warning! sc2p8 flipflop fanin 17 timing value = 0.0 for cell
/n/auspex/s15/tbr/euterpe/proteus/custom/time/tim.lib at line 83
WhatDelayType: Warning! Unknown delay type sc2p8 at line 83 for ce 11
/n/auspex/s15/tbr/euterpe/proteus/custom/time/tim.lib
```

```
Warning! sc2p3 gate fanin 17 timing value = 0.0 for cell
/n/auspex/s15/tbr/eutepe/proteus/custom/time/tim.lib at line 79
WhatDelayType: Warning! Unknown delay type sc2p3 at line 79 for ce 11
/n/auspex/s15/tbr/euterpe/proteus/custom/time/tim.lib
```

```
Warning! sc1p8 latchlatch fanin 17 timing value = 0.0 for cell
/n/auspex/s15/tb/euterpe/proteus/custom/time/tim.lib at line 75
WhatDelayType: Warning! Unknown delay type sc1p8 at line 75 for ce 11
/n/auspex/s15/tbr/euterpe/proteus/custom/time/tim.lib
```

```
Warning! sc1p3 hrflop fanin 16 timing value = 0.0 for cell
/n/auspex/s15/tbr/euerpe/proteus/custom/time/tim.lib at line 71
WhatDelayType: Warning! Unknown delay type sc1p3 at line 71 for ce 11
/n/auspex/s15/tbr/euterpe/proteus/custom/time/tim.lib
```

Tim

.

From: Lisa Robinson [lisar@nosferatu]
Sent: Thursday, September 15, 1994 1:20 AM
To: 'jeffm@nosferatu'; 'mws@nosferatu'
Cc: 'tbr@nosferatu'
Subject: sysproto1 and exmasktest

Sysproto1 Ran ok!

Dump for exmasktest is in
/a/rhodan/s3/euterpe/verilog/bsrc/exmasktest*

Lisa R.

.

From: tbr
Sent: Thursday, September 15, 1994 6:14 AM
To: 'dickson'
Subject: .splvs
Follow Up Flag: Follow up
Flag Status: Red

Please runn csyn on my bsrc/tbr_euterpe-pass1.splvs.

Tim

.

From: Mark Hofmann [hopper@cyclops]
Sent: Thursday, September 15, 1994 9:02 AM
To: 'Richard Dickson'
Cc: 'euterpe@demeter'
Subject: Re: csyn error

Richard Dickson writes:
error (OutputShortsCheck.925) in file "tbr_euterpe-pass1.splvs": net has
too many drivers

```
topmost net:
  instance path: top.xlrsltr9_8
  cellname path: top.xlrsltr9_8
drivers:
  instance path: top.xxlug_ctrltag_q_9ag_q_9a_8_72p8p_1.xlrsltr9_8
  cellname path: top.scsmf3v3 .sis1_ad1ph
  instance path: top.xxlug_ctrltag_q_9ag_q_9a_8_72p12p_1.xlrsltr9_8
  cellname path: top.scsf3v3 .d4_ad1ph
  instance path: top.xxlug_ctrltag_q_9ag_q_9a_8_72p7p_1.xlrsltr9_8
  cellname path: top.scsmf3rv3 .is3_ad1ph
topmost net:
  instance path: top.xlrsltr9_n_8
  cellname path: top.xlrsltr9_n_8
drivers:
  instance path: top.xxlug_ctrltag_q_9ag_q_9a_8_72p9p_1.xlrsltr9_n_8
  cellname path: top.scsmf3v3 .sis1_ad1ph
  instance path: top.xxlug_ctrltag_q_9ag_q_9a_8_72p10p_1.xlrsltr9_n_8
  cellname path: top.scsmf3v3 .sis1_ad1ph
  instance path: top.xxlug_ctrltag_q_9ag_q_9a_8_72p12p_1.xlrsltr9_n_8
  cellname path: top.scsf3v3 .d4_and1ph
```

no pin properties for sis1_ad1ph and is3_ad1ph in the netlist. csyn must
be assuming that one or both of these pins are outputs. csyn will guess
whether a pin is an input or an output if not given the info in netlist.

I think you've put your finger on it, Rich. sis1_ad1ph needs an input flag body.

-hopper

.

From: Mark Hofmann [hopper@cyclops]
Sent: Thursday, September 15, 1994 9:22 AM
To: 'Richard Dickson'
Cc: 'euterpe@demeter'
Subject: Re: csyn error

Richard Dickson writes:
exclusive leaf-input set

cellname path: top.scsmf3v3	.cs3a_a2peh
cellname path: top.scsmf3v3	.cs3b_a2peh
cellname path: top.scsmf3v3	.cs3c_a2peh
cellname path: top.scsmf3v3	.cs3d_a2peh
cellname path: top.scsmf3v3	.cs3e_a2peh
cellname path: top.scsmf3rv3	.zs3a_a2peh
cellname path: top.scsmf3rv3	.zs3b_a2peh
cellname path: top.scsmf3rv3	.zs3c_a2peh
cellname path: top.scsmf3rv3	.zs3d_a2peh

Looks like what's needed here is

cs3_a2peh_1
cs3_a2peh_2
cs3_a2peh_3
cs3_a2peh_4
cs3_a2peh_5

and

zs3_a2peh_1
zs3_a2peh_2
zs3_a2peh_3
zs3_a2peh_4

to satisfy the naming convention with "E" type signals.

-hopper

.

From: Mark Hofmann [hopper@cyclops]
Sent: Thursday, September 15, 1994 10:34 AM
To: 'Richard Dickson'
Cc: 'euterpe@demeter'
Subject: Re: csyn errors

Richard Dickson writes:
you'all

the output of the xlu block is _ad1ph signal type but all its destinations
are typically _ad0ph we'll have to fix this up.

Reason: drivers are non-differential or fail swing requirements.

diff inputs

instance path: top.xrgrghuopamx19ru0.xlrsltr9_83
instance path: top.xrgrghuopamx19ru0.xlrsltr9_n_83
cellname path: top.xbmux5dh3s .d2_ad0ph
cellname path: top.xbmux5dh3s .d2_and0ph

paired drivers

instance path: top.xxlug_ctrldatag_q_9ag_q_9a_19_83p3p_1.xlrsltr9_83
instance path: top.xxlug_ctrldatag_q_9ag_q_9a_19_83p1p_1.xlrsltr9_83
instance path: top.xxlug_ctrldatag_q_9ag_q_9a_19_83p4p_1.xlrsltr9_83
instance path: top.xxlug_ctrldatag_q_9ag_q_9a_19_83p6p_1.xlrsltr9_n_83
instance path: top.xxlug_ctrldatag_q_9ag_q_9a_19_83p5p_1.xlrsltr9_n_83
instance path: top.xxlug_ctrldatag_q_9ag_q_9a_19_83p1p_1.xlrsltr9_n_83
cellname path: top.scsmf3v3 .sis1_ad1ph
cellname path: top.scsf3v3 .d4_ad1ph
cellname path: top.scsmf3rv3 .is3_ad1ph
cellname path: top.scsmf3v3 .sis1_ad1ph
cellname path: top.scsmf3v3 .sis1_ad1ph
cellname path: top.scsf3v3 .d4_and1ph

paired topmost nets

instance path: top.xlrsltr9_83
instance path: top.xlrsltr9_n_83
cellname path: top.xlrsltr9_83
cellname path: top.xlrsltr9_n_83

I think these driver signals are candidates for "mp" qualifiers (signals
which can drive 0 or 1p inputs). Fred, do I have this right?

-hopper

.

From: tbr
Sent: Thursday, September 15, 1994 11:01 AM
To: 'vant'
Cc: 'geert@aphrodite'; 'hopper@aphrodite'; 'vanthof@aphrodite'
Subject: Re: timing estimator
Follow Up Flag: Follow up
Flag Status: Red

vant wrote (on Thu Sep 15):

Tim B. Robinson writes:
>
>
>Now we have the ability to set primary output strengths on an instance
>by instance basis we need some easy way to estimate what strength is
>needed. How easy would it be to come up with a script which would
>make a guess based on input say of the form:
>
><guesstime> h12s 1.3 xbmux3dh8s 2.1 xbff
>
>What I'm trying to indicate or example is: assume a half swing 12s
>output, 1.3mm wire, middle gate as specified, 2.1mm wire into a flop.
>What time would this pat have (approx)?
>
>It would need to be smart enough to handle half rate paths also.
>
>Any thoughts?
>
>Tim
>

I'm not sure I understand the above yet, but I believe something like this could be built into topt. We could set up an auxiliary file (or add something to the power.tab) which topt could read and make a guess based on the timing tables.

I had in mind something fairly simple. Just to give a better idea of what starting value to choose in the power.tab file before getting to topt. Since the lengths will be fairly gross estimates based on laying a ruler on the floorplan plot, great accuracy is not needed. Getting within 20% is probably fine. Without such a script, I'd probably assume a fixed delay for any cell for setup, clock to out or d2q, and then some lookup table for rc based on length.

Tim

From: Scott Furman [fur@quetzalcoat]
Sent: Thursday, September 15, 1994 11:24 AM
To: 'gmo@quetzalcoat'; 'abbott@quetzalcoat'; 'guarino@quetzalcoat'; 'brendan@quetzalcoat'
Subject: latest NB proposal

If the latest NB proposal (per-cylinder masks for admission control) required only SOFA changes, I think the hardware folks would grumble a bit, but would be willing to implement it. After all, the additional cost in SOFA atoms is less than 0.1 % of those on Euterpe -- it's not a make-or-break proposition.

Unfortunately, the modification to NB very probably requires a baseplate change to avoid routing a large bus from Cerberus to NB through a congested area. The baseplate is in DRC right now, a process which Tim says can take as long as a month. There doesn't seem to be a technical reason to tape-out the baseplate early - He even implied that the mask tapes would not necessarily be sent out immediately for fabrication. Rather, Tim is concerned that a delay in the baseplate tapeout would cause a later crunch for CAD licenses, machine time, and human resources.

(Given this reasoning, I'm not certain why the custom portions of the superfluous second Hermes channel aren't being removed from the baseplate right now, to reduce the apparently high risk of running out of SOFA area.)

Tim also feels that it's more important to get a functionally working chip with some deficiencies as soon as possible rather than risk delay in exchange for additional features. I agree with his sentiment, so I'm very reluctant to ask for a change to the Euterpe baseplate.

This is what I propose we ask for:

- 1) The hardware group should investigate whether there is any way to implement the new NB proposal without a baseplate change.
- 2) If there is no way to accomplish #1, it is agreed that any future change in the Euterpe baseplate will include the minor modifications to support the changes to NB. (We won't necessarily have to switch to the new NB scheme at that time. We can make the decision then as to whether we want to modify the SOFA logic and upset the verification apple-cart.)

-Scott

From: Scott Furman [fur@quetzalcoatl]
Sent: Thursday, September 15, 1994 12:20 PM
To: 'abbott (Curtis Abbott)'
Cc: 'brendan@quetzalcoatl'; 'guarino@quetzalcoatl'; 'gmo@quetzalcoatl'
Subject: latest NB proposal

Curtis Abbott writes:

> I think everything in your message is right on except >
> This is what I propose we ask for:
>
> 1) The hardware group should investigate whether there is any way
to implement the new NB proposal without a baseplate change.
>
> My problem with this is that, well, haven't they already done so (with > a lot of
stimulation from you)? Is there really something concrete > you're asking them to do?
If so, spell it out; if not, it should be > easier to get 2).
>

No, this has not been looked at, because I did not realize until yesterday that the baseplate was already in the process of tapeout.

The problem is that the change to NB is not really on the hardware group's agenda. Billz has been very cooperative and helpful, but he has made it clear that he does not like changes that enlarge, rather than shrink, NB's bounding box. I can continue to pester the hardware guys, but I think that for them to be truly motivated will require a push from Tim and hence a push on Tim from us.

-Scott

.

From: Richard Dickson [dickson@demeter]
Sent: Thursday, September 15, 1994 2:09 PM
To: 'tbr@demeter'
Subject: csyn

tim,

its alot better i'll go thru the file soon.

-rw-r--r-- 1 dickson 1298397 Sep 15 11:08 tbr_euterpe-pass1.csyn

dickson

.

From: Lisa Robinson [lisar@rhodan]
Sent: Thursday, September 15, 1994 2:09 PM
To: 'jeffm@rhodan'
Cc: 'woody@rhodan'; 'mws@rhodan'; 'tbr@rhodan'; 'billz@rhodan'
Subject: exaliagneasy

Jeff dump is in /n/rhodan/s2/euterpe/verilog/bsrc/exaligneasy.*

Lisa R.

.

From: tbr
Sent: Thursday, September 15, 1994 2:10 PM
To: 'Richard Dickson'
Subject: csyn
Follow Up Flag: Follow up
Flag Status: Red

Richard Dickson wrote (on Thu Sep 15):

tim,

its alot better i'll go thru the file soon.

-rw-r--r-- 1 dickson 1298397 Sep 15 11:08 tbr_euterpe-pass1.csyn

Great!

Tim

From: Richard Dickson [dickson@demeter]
Sent: Thursday, September 15, 1994 3:39 PM
To: 'euterpe@demeter'
Subject: csyn error

error (OutputShortsCheck.925) in file "tbr_euterpe-pass1.splvs": net has too many drivers

topmost net:

instance path: top.xlrsltr9_8
cellname path: top.xlrsltr9_8

drivers:

instance path: top.xxlug_ctrldatag_q_9ag_q_9a_8_72p8p_1.xlrsltr9_8
cellname path: top.scsmf3v3 .sis1_ad1ph
instance path: top.xxlug_ctrldatag_q_9ag_q_9a_8_72p12p_1.xlrsltr9_8
cellname path: top.scsmf3v3 .d4_ad1ph
instance path: top.xxlug_ctrldatag_q_9ag_q_9a_8_72p7p_1.xlrsltr9_8
cellname path: top.scsmf3rv3 .is3_ad1ph

topmost net:

instance path: top.xlrsltr9_n_8
cellname path: top.xlrsltr9_n_8

drivers:

instance path: top.xxlug_ctrldatag_q_9ag_q_9a_8_72p9p_1.xlrsltr9_n_8
cellname path: top.scsmf3v3 .sis1_ad1ph
instance path: top.xxlug_ctrldatag_q_9ag_q_9a_8_72p10p_1.xlrsltr9_n_8
cellname path: top.scsmf3v3 .sis1_ad1ph
instance path: top.xxlug_ctrldatag_q_9ag_q_9a_8_72p12p_1.xlrsltr9_n_8
cellname path: top.scsmf3v3 .d4_and1ph

no pin properties for sis1_ad1ph and is3_ad1ph in the netlist. csyn must be assuming that one or both of these pins are outputs. csyn will guess whether a pin is an input or an output if not given the info in netlist.

dickson

.

From: Richard Dickson [dickson@demeter]
Sent: Thursday, September 15, 1994 4:08 PM
To: 'euterpe@demeter'
Subject: csyn error

you'll

heres another one ???

error (ExclusiveInputSetCheck.227) in file "tbr_euterpe-pass1.splvs": invalid
exclusive leaf-input set

cellname path: top.scsmf3v3	.cs3a_a2peh
cellname path: top.scsmf3v3	.cs3b_a2peh
cellname path: top.scsmf3v3	.cs3c_a2peh
cellname path: top.scsmf3v3	.cs3d_a2peh
cellname path: top.scsmf3v3	.cs3e_a2peh
cellname path: top.scsmf3rv3	.zs3a_a2peh
cellname path: top.scsmf3rv3	.zs3b_a2peh
cellname path: top.scsmf3rv3	.zs3c_a2peh
cellname path: top.scsmf3rv3	.zs3d_a2peh

dickson

.

From: Lisa Robinson [lisar@rhodan]
Sent: Thursday, September 15, 1994 4:21 PM
To: 'jeffm@rhodan'
Cc: 'mws@rhodan'; 'woody@rhodan'; 'billz@rhodan'; 'tbr@rhodan'
Subject: extimertest

Dump in /n/rhodan/s3/euterpe/verilog/bsrc/extimertest.*

Lisa R.

.

From: vant [vanthof@hestia]
Sent: Thursday, September 15, 1994 4:31 PM
To: 'Tim B. Robinson'
Cc: 'Dave Van't Hof'
Subject: Re: topt nit

Tim B. Robinson writes:

>
>
>I saw the following in the .log file. There seems to be a missing
>newline:
>
>Warning! clk_to_q latch fanin 1 timing value = 0.0 for cell xbhrdf32s at line 135902
>Warning! clk_to_q hrflop fanin 1 timing value = 0.0 for cell xbhrdf32s at line 135923 Reading Cap/Delay table
file /n/auspex/s15/tbr/euterpe/proteus/custom/time/tim.lib
>Warning. Invalid format at line 10
>Warning. Invalid format at line 15
>
>Tim
>

Okey Dokey. I've put in a change for that and this version should be installed within the next 1/2 hour if I don't find anything else to change.

Thanks,
Dave

--
Dave Van't Hof vanthof@microunity.com MicroUnity Systems Engineering, Inc.
"What rolls down stairs, alone or in pairs, rolls over the neighbor's dog?
What's great for a snack and fits on your back? It's log, log, log!"
LOG from BLAMMO! (tm) All kids love Log! #include <std_disclaim.h>

From: Richard Dickson [dickson@demeter]
Sent: Thursday, September 15, 1994 4:37 PM
To: 'euterpe@demeter'
Subject: csyn errors

you'll

the output of the xlu block is _ad1ph signal type but all its destinations are typically _ad0ph we'll have to fix this up.

Reason: drivers are non-differential or fail swing requirements.

diff inputs

instance path: top.xrgrghuopamx19rru0.xlrsltr9_83
instance path: top.xrgrghuopamx19rru0.xlrsltr9_n_83
cellname path: top.xbmux5dh3s .d2_ad0ph
cellname path: top.xbmux5dh3s .d2_and0ph

paired drivers

instance path: top.xxlug_ctrldatag_q_9ag_q_9a_19_83p3p_1.xlrsltr9_83
instance path: top.xxlug_ctrldatag_q_9ag_q_9a_19_83p1p_1.xlrsltr9_83
instance path: top.xxlug_ctrldatag_q_9ag_q_9a_19_83p4p_1.xlrsltr9_83
instance path: top.xxlug_ctrldatag_q_9ag_q_9a_19_83p6p_1.xlrsltr9_n_83
instance path: top.xxlug_ctrldatag_q_9ag_q_9a_19_83p5p_1.xlrsltr9_n_83
instance path: top.xxlug_ctrldatag_q_9ag_q_9a_19_83p1p_1.xlrsltr9_n_83
cellname path: top.scsmf3v3 .sis1_ad1ph
cellname path: top.scsf3v3 .d4_ad1ph
cellname path: top.scsmf3rv3 .is3_ad1ph
cellname path: top.scsmf3v3 .sis1_ad1ph
cellname path: top.scsmf3v3 .sis1_ad1ph
cellname path: top.scsf3v3 .d4_and1ph

paired topmost nets

instance path: top.xlrsltr9_83
instance path: top.xlrsltr9_n_83
cellname path: top.xlrsltr9_83
cellname path: top.xlrsltr9_n_83

dickson

.

From: tbr
Sent: Thursday, September 15, 1994 5:02 PM
To: 'Mark Hofmann'
Cc: 'Richard Dickson'; 'vo'
Subject: Re: csyn error
Follow Up Flag: Follow up
Flag Status: Red

Can tom take care of this in bill's absense? When the change is checked in, we will need a releasebom in ged/sc to get the correct edif representatin to build. I can handle that if needed as I have the full tree checked out.

Tim

Mark Hofmann wrote (on Thu Sep 15):

Richard Dickson writes:
error (OutputShortsCheck.925) in file "tbr_euterpe-pass1.splvs": net has too many drivers

```
topmost net:
  instance path: top.xlrsltr9_8
  cellname path: top.xlrsltr9_8
drivers:
  instance path: top.xxlug_ctrldatag_q_9ag_q_9a_8_72p8p_1.xlrsltr9_8
  cellname path: top.scsmf3v3 .sis1_ad1ph
  instance path: top.xxlug_ctrldatag_q_9ag_q_9a_8_72p12p_1.xlrsltr9_8
  cellname path: top.scsmf3v3 .d4_ad1ph
  instance path: top.xxlug_ctrldatag_q_9ag_q_9a_8_72p7p_1.xlrsltr9_8
  cellname path: top.scsmf3rv3 .is3_ad1ph
topmost net:
  instance path: top.xlrsltr9_n_8
  cellname path: top.xlrsltr9_n_8
drivers:
  instance path: top.xxlug_ctrldatag_q_9ag_q_9a_8_72p9p_1.xlrsltr9_n_8
  cellname path: top.scsmf3v3 .sis1_ad1ph
  instance path: top.xxlug_ctrldatag_q_9ag_q_9a_8_72p10p_1.xlrsltr9_n_8
  cellname path: top.scsmf3v3 .sis1_ad1ph
  instance path: top.xxlug_ctrldatag_q_9ag_q_9a_8_72p12p_1.xlrsltr9_n_8
  cellname path: top.scsmf3v3 .d4_and1ph
```

no pin properties for sis1_ad1ph and is3_ad1ph in the netlist. csyn must be assuming that one or both of these pins are outputs. csyn will guess whether a pin is an input or an output if not given the info in netlist.

I think you've put your finger on it, Rich. sis1_ad1ph needs an input flag body.

-hopper

.

From: Lisa Robinson [lisar@rhodan]
Sent: Thursday, September 15, 1994 5:23 PM
To: 'jeffm@rhodan'
Cc: 'woody@rhodan'; 'mws@rhodan'; 'tbr@rhodan'
Subject: privnumtest

Dump in /n/rhodan/s3/euterpe/verilog/bsrc/privnumtest.*

Lisa R.

.

From: Fred Obermeier [fwo@pelagon]
Sent: Thursday, September 15, 1994 5:43 PM
To: 'dickson@demeter'; 'hopper@cyclops'
Cc: 'euterpe@demeter'; 'fwo@pelagon'
Subject: Re: csyn errors

> Mark sez:
> I think these driver signals are candidates for "mp" qualifiers (signals
> which can drive 0 or 1p inputs). Fred, do I have this right?

Actually, that's backwards. The range p-qualifiers are inputs, not outputs. An "mp" input can be driven by a 0p or 1p output, while an "lp" input can be driven by a 1p or 2p output. I'm not sure if these range p-qualifiers can be of help here.

Fred.

.

From: tbr
Sent: Thursday, September 15, 1994 5:53 PM
To: 'Mark Hofmann'
Cc: 'Richard Dickson'; 'euterpe@demeter'
Subject: Re: csyn errors
Follow Up Flag: Follow up
Flag Status: Red

Mark Hofmann wrote (on Thu Sep 15):

Richard Dickson writes:
you'll

the output of the xlu block is _ad1ph signal type but all its destinations are typically _ad0ph we'll have to fix this up.

Reason: drivers are non-differential or fail swing requirements.
diff inputs

instance path: top.xrgrghuopamx19rru0.xlrsltr9_83
instance path: top.xrgrghuopamx19rru0.xlrsltr9_n_83
cellname path: top.xbmux5dh3s .d2_ad0ph
cellname path: top.xbmux5dh3s .d2_and0ph

paired drivers

instance path: top.xxlug_ctrldatag_q_9ag_q_9a_19_83p3p_1.xlrsltr9_83
instance path: top.xxlug_ctrldatag_q_9ag_q_9a_19_83p1p_1.xlrsltr9_83
instance path: top.xxlug_ctrldatag_q_9ag_q_9a_19_83p4p_1.xlrsltr9_83
instance path: top.xxlug_ctrldatag_q_9ag_q_9a_19_83p6p_1.xlrsltr9_n_83
instance path: top.xxlug_ctrldatag_q_9ag_q_9a_19_83p5p_1.xlrsltr9_n_83
instance path: top.xxlug_ctrldatag_q_9ag_q_9a_19_83p1p_1.xlrsltr9_n_83
cellname path: top.scsmf3v3 .sis1_ad1ph
cellname path: top.scsof3v3 .d4_ad1ph
cellname path: top.scsmf3rv3 .is3_ad1ph
cellname path: top.scsmf3v3 .sis1_ad1ph
cellname path: top.scsmf3v3 .sis1_ad1ph
cellname path: top.scsof3v3 .d4_and1ph

paired topmost nets

instance path: top.xlrsltr9_83
instance path: top.xlrsltr9_n_83
cellname path: top.xlrsltr9_83
cellname path: top.xlrsltr9_n_83

I think these driver signals are candidates for "mp" qualifiers (signals which can drive 0 or 1p inputs). Fred, do I have this right?

No. Currently they are 1p outputs which ought to be able to drive mp inputs. However, in the design, these outputs go to xbxor3 and xbmaj3 gates which can only accept 1p inputs. So we need the XLU to have 0p outputs or we will have to have yet another rank of custom converters to get the outputs into a form our regular cells can use.

Tim

.

From: Jay Tomlinson [woody@demeter]
Sent: Thursday, September 15, 1994 10:15 PM
To: 'tbr@demeter'
Cc: 'dickson@demeter'; 'llsar@demeter'
Subject: xlu cell change doesn't compile

My local proteus is pointing to /u/chip. Do I have something set-up wrong?

Lisa I think I have a fix for the knoeasy bug, but I can't test it.

Jay

Warning! Port sizes differ in port connection (port 6) [Verilog-PCDPC]
"/n/auspex/s20/woody/chip/euterpe/proteus/verilog
/ged/scsx3pv3.v", 75: ZS3A1_AE2PH

Error! Too many module port connections [Verilog-TMPC]
"/n/auspex/s20/woody/chip/euterpe/proteus/verilog
/ged/scsx3pv3.v", 75: P4P_1(PHIA, PHIB, PHIA,
PHIB, PHIA, PHIB, ZS3A1_AE2PH, ZS3B1_AE2PH,
ZS3C1_AE2PH, ZS3D1_AE2PH, Z3B_AD1PH,
Z3B_AND1PH, Z3C_AD1PH, Z3C_AND1PH, XD3C3B0_AD1PH
, XD3C3B0_AND1PH, D4I_AD1PH, UN1SCSMF3RV34PDO210
, UN1SCSMF3RV34PDO20, UN1SCSMF3RV34PR10,
UN1SCSMF3RV34PR0)

Warning! Port sizes differ in port connection (port 6) [Verilog-PCDPC]
"/n/auspex/s20/woody/chip/euterpe/proteus/verilog
/ged/scsx3pv3.v", 80: ZS3A0_AE2PH

Error! Too many module port connections [Verilog-TMPC]
"/n/auspex/s20/woody/chip/euterpe/proteus/verilog
/ged/scsx3pv3.v", 80: P7P_1(PHIA, PHIB, PHIA,
PHIB, PHIA, PHIB, ZS3A0_AE2PH, ZS3B0_AE2PH,
ZS3C0_AE2PH, ZS3D0_AE2PH, Z3B_AD1PH,
Z3B_AND1PH, Z3C_AD1PH, Z3C_AND1PH, XD3C3A0_AD1PH
, XD3C3A0_AND1PH, D40_AD1PH, UN1SCSMF3RV37PDO210
, UN1SCSMF3RV37PDO20, UN1SCSMF3RV37PR0,
UN1SCSMF3RV37PR10)

....

Error! Maximum error count 200 exceeded. Please use
+max_err_count+<num> to modify maximum error count

gmake: *** [bsim] Error 1

.

From: tbr
Sent: Thursday, September 15, 1994 10:56 PM
To: 'Jay Tomlinson'
Cc: 'dickson@demeter'; 'lisar@demeter'
Subject: xlu cell change doesn't compile
Follow Up Flag: Follow up
Flag Status: Red

Jay Tomlinson wrote (on Thu Sep 15):

My local proteus is pointing to /u/chip. Do I have something set-up wrong?

Lisa I think I have a fix for the knobasy bug, but I can't test it.
Jay

Warning! Port sizes differ in port connection (port 6) [Verilog-PCDPC]
"/n/auspex/s20/woody/chip/euterpe/proteus/verilog
/ged/scsx3pv3.v", 75: ZS3A1_AE2PH

Error! Too many module port connections [Verilog-TMPC]
"/n/auspex/s20/woody/chip/euterpe/proteus/verilog
/ged/scsx3pv3.v", 75: P4P_1(PH1A, PH1B, PH1A,
PH1B, PH1A, PH1B, ZS3A1_AE2PH, ZS3B1_AE2PH,
ZS3C1_AE2PH, ZS3D1_AE2PH, Z3B_AD1PH,
Z3B_AND1PH, Z3C_AD1PH, Z3C_AND1PH, XD3C3B0_AD1PH
, XD3C3B0_AND1PH, D41_AD1PH, UN1SCSMF3RV34PDO210
, UN1SCSMF3RV34PDO20, UN1SCSMF3RV34PR10,
UN1SCSMF3RV34PR0)

Warning! Port sizes differ in port connection (port 6) [Verilog-PCDPC]
"/n/auspex/s20/woody/chip/euterpe/proteus/verilog
/ged/scsx3pv3.v", 80: ZS3A0_AE2PH

Error! Too many module port connections [Verilog-TMPC]
"/n/auspex/s20/woody/chip/euterpe/proteus/verilog
/ged/scsx3pv3.v", 80: P7P_1(PH1A, PH1B, PH1A,
PH1B, PH1A, PH1B, ZS3A0_AE2PH, ZS3B0_AE2PH,
ZS3C0_AE2PH, ZS3D0_AE2PH, Z3B_AD1PH,
Z3B_AND1PH, Z3C_AD1PH, Z3C_AND1PH, XD3C3A0_AD1PH
, XD3C3A0_AND1PH, D40_AD1PH, UN1SCSMF3RV37PDO210
, UN1SCSMF3RV37PDO20, UN1SCSMF3RV37PR0,
UN1SCSMF3RV37PR10)

....

Error! Maximum error count 200 exceeded. Please use
+max_err_count+<num> to modify maximum error count

gmake: *** [bsim] Error 1

No, it's a result of the release I mailed the warning about. For some

reason the rebuild in /u/chip failed when the auspex was rebooted. I'm trying to recover it now.

Tim

From: tbr
Sent: Thursday, September 15, 1994 11:29 PM
To: 'vant'
Cc: 'Dave Van't Hof'
Subject: Re: pager log message
Follow Up Flag: Follow up
Flag Status: Red

vant wrote (on Thu Sep 15):

Tim B. Robinson writes:
>
>page from tbr to vanthof.
>With latest topt now having trouble with regular flops mismatching pincount. tbr
>
>

Hi. What module are you having problems with?

rg. here's a sample:

... Processing rest of user PDL.
In XBORFF3DH24S at line 13795:
--> NPINS:10;

!
** Syntax Error: The number of pins on the logical type XBORFF3DH24S
(NPINS = 12) does not agree with the corresponding physical type
XBORFF3DH24S (NPINS = 10).
(Message number 5 Severity 5)

In XBORFF5DH24S at line 14337:
--> NPINS:12;

!
** Syntax Error: The number of pins on the logical type XBORFF5DH24S
(NPINS = 14) does not agree with the corresponding physical type
XBORFF5DH24S (NPINS = 12).
(Message number 5 Severity 5)

... Processing rest of system PDL.
... Processing TDL.
... TECHNOLOGYLIB:SOFA;
... Computed Grid_Size = 1000
... Final Processing.

2 fatal errors occurred. PCOMP aborting.

Terminated at : 94/09/15 21:18:59
Elapsed CPU time : 0 Hrs 0 Mins 5 Secs
Elapsed wall clock time : 0 Hrs 0 Mins 6 Secs
make[2]: *** [gards/rg-pass2.pcomp.lis] Error 1
make[2]: Leaving directory '/N/auspex/root/s15/tbr/euterpe/verilog/bsrc/rg'
make[1]: *** [rg-base.netcap] Error 1

```
rm rgplr0.optesp rgplr0.esp
make[1]: Leaving directory `/N/auspex/root/s15/tbr/euterpe/verilog/bsrc/rg'
make: *** [rggards] Error 1
```

Pass 1 was fine.

Tim

.

From: tbr
Sent: Thursday, September 15, 1994 11:35 PM
To: 'dickson'
Subject: euterpe_driver.V
Follow Up Flag: Follow up
Flag Status: Red

What is the force of "burst"? In the system we have to rely on cerberus coming up without anything external holding SD down initially.

Tim

From: vant [vanthof@hestia]
Sent: Friday, September 16, 1994 12:11 AM
To: 'Geert Rosseel'
Cc: 'Dave Van't Hof'; 'Mark Hofmann'; 'Tim B. Robinson'
Subject: topt return code when running on euterpe

Geert,

I can't duplicate the topt return code of 4 which you were seeing when running on euterpe. I'll keep look as hopper is also seeing the BAD EDIF return code, but I'm confused.

Thanks,
Dave

--

Dave Van't Hof vanthof@microunity.com MicroUnity Systems Engineering,
Inc.

"What rolls down stairs, alone or in pairs, rolls over the neighbor's dog?"

What's great for a snack and fits on your back? It's log, log, log!"
LOG from BLAMMO! (tm) All kids love Log! #include
<std_disclaim.h>

From: Richard Dickson [dickson@gamorra]
Sent: Friday, September 16, 1994 12:30 AM
To: 'euterpe@gamorra'
Subject: csyn error

you'all

heres another one

```
input
  instance path: top.xpadbl.nc46
  cellname path: top.padbl .pmosg_v
topmost net
  instance path: top.nc46
  cellname path: top.nc46

input
  instance path: top.xpadbr.nc49
  cellname path: top.padbr .bjt1b_v
topmost net
  instance path: top.nc49
  cellname path: top.nc49

input
  instance path: top.xpadtl.nc41
  cellname path: top.padt1 .nmosg_v
topmost net
  instance path: top.nc41
  cellname path: top.nc41

input
  instance path: top.xpadtr.nc43
  cellname path: top.padtr .r2kwl_v
topmost net
  instance path: top.nc43
  cellname path: top.nc43
```

dickson

.

From: Richard Dickson [dickson@demeter]
Sent: Friday, September 16, 1994 1:09 AM
To: 'tbr@demeter'
Subject: gards/topt

tim,

i,ve been updating pim files and re-running a couple
gards blocks (mc and gf) they both fail in this way.

Memory usage: 29,301MB
Exit code: 3 (Invalid Input Data)
gmake[1]: *** [mc-iter] Error 1
gmake[1]: Leaving directory `/N/rama/root/s5/dickson/euterpe/verilog/bsrc/mc'
gmake: *** [mcgards] Error 1

does this mean topt ran across some bad timing data ?

dickson

.

From: tbr
Sent: Friday, September 16, 1994 1:12 AM
To: 'Richard Dickson'
Subject: gards/topt
Follow Up Flag: Follow up
Flag Status: Red

Richard Dickson wrote (on Thu Sep 15):

tim,

i,ve been updating pim files and re-running a couple
gards blocks (mc and gf) they both fail in this way.

Memory usage: 29.301MB
Exit code: 3 (Invalid Input Data)
gmake[1]: *** [mc-iter] Error 1
gmake[1]: Leaving directory `/N/rama/root/s5/dickson/euterpe/verilog/bsrc/mc'
gmake: *** [mcgards] Error 1

does this mean topt ran across some bad timing data ?

Possibly. forward to dave. He's been trying to track down soem
problem geert and hopper were seeing. This may be related.

I'm currently seeing another problem in that the number of clockinputs
on the flops are getting messed up.

Tim

.

From: Lisa Robinson [lisar@nosferatu]
Sent: Friday, September 16, 1994 1:26 AM
To: 'jeffm@nosferatu'
Cc: 'woody@nosferatu'; 'billz@nosferatu'; 'mws@nosferatu'; 'tbr@nosferatu'
Subject: exaligntest failed

Fairly early - register commit trace in
/n/nosferatu/s2/euterpe/verilog/bsrc/rs/15994.109/results/exaligntest.dpo.

Blink and extimertest ran ok.

Lisa R.

.

From: vant [vanthof@hestia]
Sent: Friday, September 16, 1994 1:26 AM
To: 'Tim B. Robinson'
Cc: 'Dave Van't Hof'; 'Mark Hofmann'
Subject: Re: pager log message

Tim B. Robinson writes:
>
>vant wrote (on Thu Sep 15):
>
> Tim B. Robinson writes:
> >
> >page from tbr to vanthof:
> >With latest topt now having trouble with regular flops mismatching pincount. tbr
> >
> >
> Hi. What module are you having problems with?
>
>
>rg. here's a sample:
>
>... Processing rest of user PDL.
>In XBORFF3DH24S at line 13795:
>--> NPINS:10;
> !
>** Syntax Error: The number of pins on the logical type XBORFF3DH24S
>(NPINS = 12) does not agree with the corresponding physical type
>XBORFF3DH24S (NPINS = 10).
>(Message number 5 Severity 5)
>
>In XBORFF5DH24S at line 14337:
>--> NPINS:12;
> !
>** Syntax Error: The number of pins on the logical type XBORFF5DH24S
>(NPINS = 14) does not agree with the corresponding physical type
>XBORFF5DH24S (NPINS = 12).
>(Message number 5 Severity 5)
>
>... Processing rest of system PDL.
>... Processing TDL.
>... TECHNOLOGYLIB:SOFA;
>... Computed Grid_Size = 1000
>... Final Processing.
>
> 2 fatal errors occurred. PCOMP aborting.
>
>Terminated at : 94/09/15 21:18:59
>Elapsed CPU time : 0 Hrs 0 Mins 5 Secs
>Elapsed wall clock time : 0 Hrs 0 Mins 6 Secs
>make[2]: *** [gards/rg-pass2.pcomp.lis] Error 1
>make[2]: Leaving directory '/N/auspex/root/s15/tbr/euterpe/verilog/bsrc/rg'
>make[1]: *** [rg-base.netcap] Error 1
>rm rgplr0.optesp rgplr0.esp
>make[1]: Leaving directory '/N/auspex/root/s15/tbr/euterpe/verilog/bsrc/rg'

```
>make: *** [rggards] Error 1
>
>
>Pass 1 was fine.
>
>Tim
>
```

Okay. please try again. I found a problem with powering primary outputs because of this 2p stuff.

Sorry about that.
Dave

--

Dave Van't Hof vanthof@microunity.com MicroUnity Systems Engineering, Inc.
"What rolls down stairs, alone or in pairs, rolls over the neighbor's dog?
What's great for a snack and fits on your back? It's log, log, log!"
LOG from BLAMMO! (tm) All kids love Log! #include <std_disclaim.h>

.

From: tbr
Sent: Friday, September 16, 1994 8:11 AM
To: 'vanthof'
Subject: Exit status 4
Follow Up Flag: Follow up
Flag Status: Red

It happend for me with your latest version. I was runnint
tbr_euterpe-pass1 in my bsrc directory.

I have not looked over the log file, but will when I get in.

Tim

.

From: vant [vanthof@hestia]
Sent: Friday, September 16, 1994 8:12 AM
To: 'Tim B. Robinson'
Cc: 'vanthof@aphrodite'
Subject: Re: Exit status 4

Tim B. Robinson writes:

>
>
>It happend for me with your latest version. I was runnint
>tbr_euterpe-pass1 in my bsrc directory.
>
>I have not looked over the log file, but will when I get in.
>
>Tim
>

Okay. I'll take a look. Something somewhere is setting this and I can't seem to find it.

Thanks,
Dave

--
Dave Van't Hof vanthof@microunity.com MicroUnity Systems Engineering, Inc.
"What rolls down stairs, alone or in pairs, rolls over the neighbor's dog?
What's great for a snack and fits on your back? It's log, log, log!"
LOG from BLAMMO! (tm) All kids love Log! #include <std_disclaim.h>

.

From: tbr
Sent: Friday, September 16, 1994 10:50 AM
To: 'doi'
Subject: releasebom
Follow Up Flag: Follow up
Flag Status: Red

There is a problem when a releasebom happens in a lower level and the non .0 bom is created at higher levels. The log message for the upper level BOM does not show what subdir caused it. eg in euterpe/verilog/bsrc:

revision 119.8
date: 1994/09/15 21:32:11 LT; author: tbr; state: Exp; lines: +2 -2
updated power.tab.local

revision 119.7
date: 1994/09/15 21:30:00 LT; author: tbr; state: Exp; lines: +2 -2
latest placement

The messages are meaningful in the section where they were entered, but convey nothing at the top level. Is it possible to add something to this log to say which sub-dir the message came from?

Tim

.

From: tbr
Sent: Friday, September 16, 1994 11:04 AM
To: 'geert'; 'hopper'
Cc: 'vanthof'
Subject: Bogus data
Follow Up Flag: Follow up
Flag Status: Red

This lot came back in one of my runs last night:

WhatDelayType: Warning! Unknown delay type iobyte at line 62 for ce
ll iobyte

Warning! iobyte gate fanin 1 timing value = 0.0 for cell iobyte at line 62
WhatDelayType: Warning! Unknown delay type iobyte at line 62 for ce
ll iobyte

Warning! iobyte latch fanin 1 timing value = 0.0 for cell iobyte at line 62
WhatDelayType: Warning! Unknown delay type iobyte at line 62 for ce
ll iobyte

Warning! iobyte flipflop fanin 1 timing value = 0.0 for cell iobyte at line 62
WhatDelayType: Warning! Unknown delay type iobyte at line 62 for ce
ll iobyte

Warning! iobyte latchlatch fanin 1 timing value = 0.0 for cell iobyte at line 62
WhatDelayType: Warning! Unknown delay type iobyte at line 62 for ce
ll iobyte

Warning! iobyte hrflop fanin 1 timing value = 0.0 for cell iobyte at line 62
WhatDelayType: Warning! Unknown delay type iobyte at line 62 for ce
ll iobyte

Warning! iobyte gate fanin 2 timing value = 0.0 for cell iobyte at line 62
WhatDelayType: Warning! Unknown delay type iobyte at line 62 for ce
ll iobyte

Warning! iobyte latch fanin 2 timing value = 0.0 for cell iobyte at line 62
WhatDelayType: Warning! Unknown delay type iobyte at line 62 for ce
ll iobyte

Warning! iobyte flipflop fanin 2 timing value = 0.0 for cell iobyte at line 62
WhatDelayType: Warning! Unknown delay type iobyte at line 62 for ce
ll iobyte

Warning! iobyte latchlatch fanin 2 timing value = 0.0 for cell iobyte at line 62
WhatDelayType: Warning! Unknown delay type iobyte at line 62 for ce
ll iobyte

Warning! iobyte hrflop fanin 2 timing value = 0.0 for cell iobyte at line 62
WhatDelayType: Warning! Unknown delay type iobyte at line 62 for ce
ll iobyte

Warning! iobyte gate fanin 3 timing value = 0.0 for cell iobyte at line 62
WhatDelayType: Warning! Unknown delay type iobyte at line 62 for ce
ll iobyte

Warning! iobyte latch fanin 3 timing value = 0.0 for cell iobyte at line 62
WhatDelayType: Warning! Unknown delay type iobyte at line 62 for ce
ll iobyte

Warning! iobyte flipflop fanin 3 timing value = 0.0 for cell iobyte at line 62
WhatDelayType: Warning! Unknown delay type iobyte at line 62 for ce
ll iobyte

Warning! iobyte latchlatch fanin 3 timing value = 0.0 for cell iobyte at line 62
WhatDelayType: Warning! Unknown delay type iobyte at line 62 for ce
ll iobyte

Warning! iobyte hrflop fanin 3 timing value = 0.0 for cell iobyte at line 62
WhatDelayType: Warning! Unknown delay type iobyte at line 62 for ce
ll iobyte

Warning! iobyte gate fanin 4 timing value = 0.0 for cell iobyte at line 62
WhatDelayType: Warning! Unknown delay type iobyte at line 62 for ce
ll iobyte

Warning! iobyte latch fanin 4 timing value = 0.0 for cell iobyte at line 62
WhatDelayType: Warning! Unknown delay type iobyte at line 62 for ce
ll iobyte

Warning! iobyte flipflop fanin 4 timing value = 0.0 for cell iobyte at line 62
WhatDelayType: Warning! Unknown delay type iobyte at line 62 for ce
ll iobyte

Warning! iobyte latchlatch fanin 4 timing value = 0.0 for cell iobyte at line 62
WhatDelayType: Warning! Unknown delay type iobyte at line 62 for ce
ll iobyte

Warning! iobyte hrflop fanin 4 timing value = 0.0 for cell iobyte at line 62
WhatDelayType: Warning! Unknown delay type iobyte at line 62 for ce
ll iobyte

Warning! iobyte gate fanin 5 timing value = 0.0 for cell iobyte at line 62
WhatDelayType: Warning! Unknown delay type iobyte at line 62 for ce
ll iobyte

Warning! iobyte latch fanin 5 timing value = 0.0 for cell iobyte at line 62
WhatDelayType: Warning! Unknown delay type iobyte at line 62 for ce
ll iobyte

Warning! iobyte flipflop fanin 5 timing value = 0.0 for cell iobyte at line 62
WhatDelayType: Warning! Unknown delay type iobyte at line 62 for ce
ll iobyte

Warning! iobyte latchlatch fanin 5 timing value = 0.0 for cell iobyte at line 62
WhatDelayType: Warning! Unknown delay type iobyte at line 62 for ce
ll iobyte

Warning! iobyte hrflop fanin 5 timing value = 0.0 for cell iobyte at line 62
WhatDelayType: Warning! Unknown delay type iobyte at line 62 for ce
ll iobyte

Warning! iobyte gate fanin 6 timing value = 0.0 for cell iobyte at line 62
WhatDelayType: Warning! Unknown delay type iobyte at line 62 for ce
ll iobyte

Warning! iobyte latch fanin 6 timing value = 0.0 for cell iobyte at line 62
WhatDelayType: Warning! Unknown delay type iobyte at line 62 for ce
ll iobyte

Warning! iobyte flipflop fanin 6 timing value = 0.0 for cell iobyte at line 62
WhatDelayType: Warning! Unknown delay type iobyte at line 62 for ce
ll iobyte

Warning! iobyte latchlatch fanin 6 timing value = 0.0 for cell iobyte at line 62
WhatDelayType: Warning! Unknown delay type iobyte at line 62 for ce
ll iobyte

Warning! iobyte hrflop fanin 6 timing value = 0.0 for cell iobyte at line 62
WhatDelayType: Warning! Unknown delay type iobyte at line 62 for ce
ll iobyte

Warning! iobyte gate fanin 7 timing value = 0.0 for cell iobyte at line 62
WhatDelayType: Warning! Unknown delay type iobyte at line 62 for ce
ll iobyte

Warning! iobyte latch fanin 7 timing value = 0.0 for cell iobyte at line 62
WhatDelayType: Warning! Unknown delay type iobyte at line 62 for ce
ll iobyte

Warning! iobyte flipflop fanin 7 timing value = 0.0 for cell iobyte at line 62
WhatDelayType: Warning! Unknown delay type iobyte at line 62 for ce
ll iobyte

Warning! iobyte latchlatch fanin 7 timing value = 0.0 for cell iobyte at line 62
WhatDelayType: Warning! Unknown delay type iobyte at line 62 for ce
ll iobyte

Warning! iobyte hrflop fanin 7 timing value = 0.0 for cell iobyte at line 62
WhatDelayType: Warning! Unknown delay type iobyte at line 62 for ce
ll iobyte

Warning! iobyte gate fanin 8 timing value = 0.0 for cell iobyte at line 62
WhatDelayType: Warning! Unknown delay type iobyte at line 62 for ce
ll iobyte

Warning! iobyte latch fanin 8 timing value = 0.0 for cell iobyte at line 62
WhatDelayType: Warning! Unknown delay type iobyte at line 62 for ce
ll iobyte

Warning! iobyte flipflop fanin 8 timing value = 0.0 for cell iobyte at line 62
WhatDelayType: Warning! Unknown delay type iobyte at line 62 for ce
ll iobyte

Warning! iobyte latchlatch fanin 8 timing value = 0.0 for cell iobyte at line 62
WhatDelayType: Warning! Unknown delay type iobyte at line 62 for ce
ll iobyte

Warning! iobyte hrflop fanin 8 timing value = 0.0 for cell iobyte at line 62
WhatDelayType: Warning! Unknown delay type iobyte at line 62 for ce
ll iobyte

Warning! iobyte gate fanin 9 timing value = 0.0 for cell iobyte at line 62

WhatDelayType: Warning! Unknown delay type iobyte at line 62 for ce
ll iobyte

Warning! iobyte latch fanin 9 timing value = 0.0 for cell iobyte at line 62
WhatDelayType: Warning! Unknown delay type iobyte at line 62 for ce
ll iobyte

Warning! iobyte flipflop fanin 9 timing value = 0.0 for cell iobyte at line 62
WhatDelayType: Warning! Unknown delay type iobyte at line 62 for ce
ll iobyte

Warning! iobyte latchlatch fanin 9 timing value = 0.0 for cell iobyte at line 62
WhatDelayType: Warning! Unknown delay type iobyte at line 62 for ce
ll iobyte

Warning! iobyte hrflop fanin 9 timing value = 0.0 for cell iobyte at line 62
WhatDelayType: Warning! Unknown delay type iobyte at line 62 for ce
ll iobyte

Warning! iobyte gate fanin 10 timing value = 0.0 for cell iobyte at line 62
WhatDelayType: Warning! Unknown delay type iobyte at line 62 for ce
ll iobyte

Warning! iobyte latch fanin 10 timing value = 0.0 for cell iobyte at line 62
WhatDelayType: Warning! Unknown delay type iobyte at line 62 for ce
ll iobyte

Warning! iobyte flipflop fanin 10 timing value = 0.0 for cell iobyte at line 62
WhatDelayType: Warning! Unknown delay type iobyte at line 62 for ce
ll iobyte

Warning! iobyte latchlatch fanin 10 timing value = 0.0 for cell iobyte at line 62
WhatDelayType: Warning! Unknown delay type iobyte at line 62 for ce
ll iobyte

Warning! iobyte hrflop fanin 10 timing value = 0.0 for cell iobyte at line 62
WhatDelayType: Warning! Unknown delay type iobyte at line 62 for ce
ll iobyte

Warning! iobyte gate fanin 11 timing value = 0.0 for cell iobyte at line 62
WhatDelayType: Warning! Unknown delay type iobyte at line 62 for ce
ll iobyte

Warning! iobyte latch fanin 11 timing value = 0.0 for cell iobyte at line 62
WhatDelayType: Warning! Unknown delay type iobyte at line 62 for ce
ll iobyte

Warning! iobyte flipflop fanin 11 timing value = 0.0 for cell iobyte at line 62
WhatDelayType: Warning! Unknown delay type iobyte at line 62 for ce
ll iobyte

Warning! iobyte latchlatch fanin 11 timing value = 0.0 for cell iobyte at line 62
WhatDelayType: Warning! Unknown delay type iobyte at line 62 for ce
ll iobyte

Warning! iobyte hrflop fanin 11 timing value = 0.0 for cell iobyte at line 62
WhatDelayType: Warning! Unknown delay type iobyte at line 62 for ce
ll iobyte

Warning! iobyte gate fanin 12 timing value = 0.0 for cell iobyte at line 62
WhatDelayType: Warning! Unknown delay type iobyte at line 62 for ce

ll iobyte

Warning! iobyte latch fanin 12 timing value = 0.0 for cell iobyte at line 62
WhatDelayType: Warning! Unknown delay type iobyte at line 62 for ce
ll iobyte

Warning! iobyte flipflop fanin 12 timing value = 0.0 for cell iobyte at line 62
WhatDelayType: Warning! Unknown delay type iobyte at line 62 for ce
ll iobyte

Warning! iobyte latchlatch fanin 12 timing value = 0.0 for cell iobyte at line 62
WhatDelayType: Warning! Unknown delay type iobyte at line 62 for ce
ll iobyte

Warning! iobyte hrflop fanin 12 timing value = 0.0 for cell iobyte at line 62
WhatDelayType: Warning! Unknown delay type iobyte at line 62 for ce
ll iobyte

Warning! iobyte gate fanin 13 timing value = 0.0 for cell iobyte at line 62
WhatDelayType: Warning! Unknown delay type iobyte at line 62 for ce
ll iobyte

Warning! iobyte latch fanin 13 timing value = 0.0 for cell iobyte at line 62
WhatDelayType: Warning! Unknown delay type iobyte at line 62 for ce
ll iobyte

Warning! iobyte flipflop fanin 13 timing value = 0.0 for cell iobyte at line 62
WhatDelayType: Warning! Unknown delay type iobyte at line 62 for ce
ll iobyte

Warning! iobyte latchlatch fanin 13 timing value = 0.0 for cell iobyte at line 62
WhatDelayType: Warning! Unknown delay type iobyte at line 62 for ce
ll iobyte

Warning! iobyte hrflop fanin 13 timing value = 0.0 for cell iobyte at line 62
WhatDelayType: Warning! Unknown delay type iobyte at line 62 for ce
ll iobyte

Warning! iobyte gate fanin 14 timing value = 0.0 for cell iobyte at line 62
WhatDelayType: Warning! Unknown delay type iobyte at line 62 for ce
ll iobyte

Warning! iobyte latch fanin 14 timing value = 0.0 for cell iobyte at line 62
WhatDelayType: Warning! Unknown delay type iobyte at line 62 for ce
ll iobyte

Warning! iobyte flipflop fanin 14 timing value = 0.0 for cell iobyte at line 62
WhatDelayType: Warning! Unknown delay type iobyte at line 62 for ce
ll iobyte

Warning! iobyte latchlatch fanin 14 timing value = 0.0 for cell iobyte at line 62
WhatDelayType: Warning! Unknown delay type iobyte at line 62 for ce
ll iobyte

Warning! iobyte hrflop fanin 14 timing value = 0.0 for cell iobyte at line 62
WhatDelayType: Warning! Unknown delay type iobyte at line 62 for ce
ll iobyte

Warning! iobyte gate fanin 15 timing value = 0.0 for cell iobyte at line 62
WhatDelayType: Warning! Unknown delay type iobyte at line 62 for ce
ll iobyte

Warning! iobyte latch fanin 15 timing value = 0.0 for cell iobyte at line 62
WhatDelayType: Warning! Unknown delay type iobyte at line 62 for ce
ll iobyte

Warning! iobyte flipflop fanin 15 timing value = 0.0 for cell iobyte at line 62
WhatDelayType: Warning! Unknown delay type iobyte at line 62 for ce
ll iobyte

Warning! iobyte latchlatch fanin 15 timing value = 0.0 for cell iobyte at line 62
WhatDelayType: Warning! Unknown delay type iobyte at line 62 for ce
ll iobyte

Warning! iobyte hrflop fanin 15 timing value = 0.0 for cell iobyte at line 62
WhatDelayType: Warning! Unknown delay type iobyte at line 62 for ce
ll iobyte

Warning! iobyte gate fanin 16 timing value = 0.0 for cell iobyte at line 62
WhatDelayType: Warning! Unknown delay type iobyte at line 62 for ce
ll iobyte

Warning! iobyte latch fanin 16 timing value = 0.0 for cell iobyte at line 62
WhatDelayType: Warning! Unknown delay type iobyte at line 62 for ce
ll iobyte

Warning! iobyte flipflop fanin 16 timing value = 0.0 for cell iobyte at line 62
WhatDelayType: Warning! Unknown delay type iobyte at line 62 for ce
ll iobyte

Warning! iobyte latchlatch fanin 16 timing value = 0.0 for cell iobyte at line 62
WhatDelayType: Warning! Unknown delay type iobyte at line 62 for ce
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Warning! sc1p3 latchlatch fanin 13 timing value = 0.0 for cell sc1p3 at line 97
WhatDelayType: Warning! Unknown delay type sc1p3 at line 97 for ce
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Warning! sc1p3 hrflop fanin 13 timing value = 0.0 for cell sc1p3 at line 97
WhatDelayType: Warning! Unknown delay type sc1p3 at line 97 for ce
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Warning! sc1p3 gate fanin 14 timing value = 0.0 for cell sc1p3 at line 97
WhatDelayType: Warning! Unknown delay type sc1p3 at line 97 for ce
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Warning! sc1p3 latch fanin 14 timing value = 0.0 for cell sc1p3 at line 97
WhatDelayType: Warning! Unknown delay type sc1p3 at line 97 for ce
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Warning! sc1p3 flipflop fanin 14 timing value = 0.0 for cell sc1p3 at line 97
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Warning! sc1p3 latchlatch fanin 14 timing value = 0.0 for cell sc1p3 at line 97
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Warning! sc1p3 hrflop fanin 14 timing value = 0.0 for cell sc1p3 at line 97
WhatDelayType: Warning! Unknown delay type sc1p3 at line 97 for ce
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Warning! sc1p3 gate fanin 15 timing value = 0.0 for cell sc1p3 at line 97
WhatDelayType: Warning! Unknown delay type sc1p3 at line 97 for ce
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Warning! sc1p3 latch fanin 15 timing value = 0.0 for cell sc1p3 at line 97
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Warning! sc1p3 flipflop fanin 15 timing value = 0.0 for cell sc1p3 at line 97
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Warning! sc1p3 latchlatch fanin 15 timing value = 0.0 for cell sc1p3 at line 97
WhatDelayType: Warning! Unknown delay type sc1p3 at line 97 for ce
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Warning! sc1p3 hrflop fanin 15 timing value = 0.0 for cell sc1p3 at line 97
WhatDelayType: Warning! Unknown delay type sc1p3 at line 97 for ce
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Warning! sc1p3 gate fanin 16 timing value = 0.0 for cell sc1p3 at line 97
WhatDelayType: Warning! Unknown delay type sc1p3 at line 97 for ce
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Warning! sc1p3 latch fanin 16 timing value = 0.0 for cell sc1p3 at line 97
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Warning! sc1p3 flipflop fanin 16 timing value = 0.0 for cell sc1p3 at line 97
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Warning! sc1p3 latchlatch fanin 16 timing value = 0.0 for cell sc1p3 at line 97
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Warning! sc1p3 hrflop fanin 16 timing value = 0.0 for cell sc1p3 at line 97
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Warning! sc1p3 gate fanin 17 timing value = 0.0 for cell sc1p3 at line 97
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Warning! sc1p3 latch fanin 17 timing value = 0.0 for cell sc1p3 at line 97
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Warning! sc1p3 flipflop fanin 17 timing value = 0.0 for cell sc1p3 at line 97
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Warning! sc1p3 latchlatch fanin 17 timing value = 0.0 for cell sc1p3 at line 97
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Warning! sc1p3 hrflop fanin 17 timing value = 0.0 for cell sc1p3 at line 97
WhatDelayType: Warning! Unknown delay type sc1p8 at line 102 for cell sc1p3

Warning! sc1p8 gate fanin 1 timing value = 0.0 for cell sc1p3 at line 102
WhatDelayType: Warning! Unknown delay type sc1p8 at line 102 for cell sc1p3

Warning! sc1p8 latch fanin 1 timing value = 0.0 for cell sc1p3 at line 102
WhatDelayType: Warning! Unknown delay type sc1p8 at line 102 for cell sc1p3

Warning! sc1p8 flipflop fanin 1 timing value = 0.0 for cell sc1p3 at line 102
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Warning! sc1p8 latchlatch fanin 1 timing value = 0.0 for cell sc1p3 at line 102
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Warning! sc1p8 hrflop fanin 1 timing value = 0.0 for cell sc1p3 at line 102
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Warning! sc1p8 gate fanin 2 timing value = 0.0 for cell sc1p3 at line 102
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Warning! sc1p8 flipflop fanin 2 timing value = 0.0 for cell sc1p3 at line 102
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Warning! sc1p8 latchlatch fanin 2 timing value = 0.0 for cell sc1p3 at line 102
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Warning! sc1p8 hrflop fanin 2 timing value = 0.0 for cell sc1p3 at line 102
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Warning! sc1p8 gate fanin 3 timing value = 0.0 for cell sc1p3 at line 102
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Warning! sc1p8 latch fanin 3 timing value = 0.0 for cell sc1p3 at line 102
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Warning! sc1p8 flipflop fanin 3 timing value = 0.0 for cell sc1p3 at line 102
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Warning! sc1p8 gate fanin 4 timing value = 0.0 for cell sc1p3 at line 102
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Warning! sc1p8 flipflop fanin 4 timing value = 0.0 for cell sc1p3 at line 102
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Warning! sc1p8 gate fanin 6 timing value = 0.0 for cell sc1p3 at line 102
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Warning! sc1p8 flipflop fanin 6 timing value = 0.0 for cell sc1p3 at line 102
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Warning! sc1p8 latchlatch fanin 6 timing value = 0.0 for cell sc1p3 at line 102
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Warning! sc1p8 hrflop fanin 6 timing value = 0.0 for cell sc1p3 at line 102

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Warning! sc1p8 gate fanin 7 timing value = 0.0 for cell sc1p3 at line 102
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Warning! sc1p8 latch fanin 7 timing value = 0.0 for cell sc1p3 at line 102
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Warning! sc1p8 flipflop fanin 7 timing value = 0.0 for cell sc1p3 at line 102
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Warning! sc1p8 latchlatch fanin 7 timing value = 0.0 for cell sc1p3 at line 102
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Warning! sc1p8 hrflop fanin 7 timing value = 0.0 for cell sc1p3 at line 102
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Warning! sc1p8 gate fanin 8 timing value = 0.0 for cell sc1p3 at line 102
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Warning! sc1p8 latch fanin 8 timing value = 0.0 for cell sc1p3 at line 102
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Warning! sc1p8 flipflop fanin 8 timing value = 0.0 for cell sc1p3 at line 102
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Warning! sc1p8 latchlatch fanin 8 timing value = 0.0 for cell sc1p3 at line 102
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Warning! sc1p8 hrflop fanin 8 timing value = 0.0 for cell sc1p3 at line 102
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Warning! sc1p8 gate fanin 9 timing value = 0.0 for cell sc1p3 at line 102
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Warning! sc1p8 latch fanin 9 timing value = 0.0 for cell sc1p3 at line 102
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Warning! sc1p8 flipflop fanin 9 timing value = 0.0 for cell sc1p3 at line 102
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Warning! sc1p8 latchlatch fanin 9 timing value = 0.0 for cell sc1p3 at line 102
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Warning! sc1p8 hrflop fanin 9 timing value = 0.0 for cell sc1p3 at line 102
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Warning! sc1p8 gate fanin 10 timing value = 0.0 for cell sc1p3 at line 102
WhatDelayType: Warning! Unknown delay type sc1p8 at line 102 for ce
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Warning! sc1p8 latch fanin 10 timing value = 0.0 for cell sc1p3 at line 102
WhatDelayType: Warning! Unknown delay type sc1p8 at line 102 for ce
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Warning! sc1p8 flipflop fanin 10 timing value = 0.0 for cell sc1p3 at line 102
WhatDelayType: Warning! Unknown delay type sc1p8 at line 102 for ce
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Warning! sc1p8 latchlatch fanin 10 timing value = 0.0 for cell sc1p3 at line 102
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Warning! sc1p8 hrflop fanin 10 timing value = 0.0 for cell sc1p3 at line 102
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Warning! sc1p8 gate fanin 11 timing value = 0.0 for cell sc1p3 at line 102
WhatDelayType: Warning! Unknown delay type sc1p8 at line 102 for ce
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Warning! sc1p8 latch fanin 11 timing value = 0.0 for cell sc1p3 at line 102
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Warning! sc1p8 flipflop fanin 11 timing value = 0.0 for cell sc1p3 at line 102
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Warning! sc1p8 latchlatch fanin 11 timing value = 0.0 for cell sc1p3 at line 102
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Warning! sc1p8 hrflop fanin 11 timing value = 0.0 for cell sc1p3 at line 102
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Warning! sc1p8 gate fanin 12 timing value = 0.0 for cell sc1p3 at line 102
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Warning! sc1p8 latch fanin 12 timing value = 0.0 for cell sc1p3 at line 102
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Warning! sc1p8 flipflop fanin 12 timing value = 0.0 for cell sc1p3 at line 102
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Warning! sc1p8 latchlatch fanin 12 timing value = 0.0 for cell sc1p3 at line 102
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Warning! sc1p8 hrflop fanin 12 timing value = 0.0 for cell sc1p3 at line 102
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Warning! sc1p8 gate fanin 13 timing value = 0.0 for cell sc1p3 at line 102
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Warning! sc1p8 latch fanin 13 timing value = 0.0 for cell sc1p3 at line 102
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Warning! sc1p8 flipflop fanin 13 timing value = 0.0 for cell sc1p3 at line 102
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Warning! sc1p8 latchlatch fanin 13 timing value = 0.0 for cell sc1p3 at line 102
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Warning! sc1p8 hrflop fanin 13 timing value = 0.0 for cell sc1p3 at line 102
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Warning! sc1p8 gate fanin 14 timing value = 0.0 for cell sc1p3 at line 102
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Warning! sc1p8 latch fanin 14 timing value = 0.0 for cell sc1p3 at line 102
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Warning! sc1p8 flipflop fanin 14 timing value = 0.0 for cell sc1p3 at line 102
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Warning! sc1p8 latchlatch fanin 14 timing value = 0.0 for cell sc1p3 at line 102
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Warning! sc1p8 hrflop fanin 14 timing value = 0.0 for cell sc1p3 at line 102
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Warning! sc1p8 gate fanin 15 timing value = 0.0 for cell sc1p3 at line 102
WhatDelayType: Warning! Unknown delay type sc1p8 at line 102 for ce
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Warning! sc1p8 latch fanin 15 timing value = 0.0 for cell sc1p3 at line 102
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Warning! sc1p8 flipflop fanin 15 timing value = 0.0 for cell sc1p3 at line 102
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Warning! sc1p8 latchlatch fanin 15 timing value = 0.0 for cell sc1p3 at line 102
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Warning! sc1p8 hrflop fanin 15 timing value = 0.0 for cell sc1p3 at line 102
WhatDelayType: Warning! Unknown delay type sc1p8 at line 102 for ce
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Warning! sc1p8 gate fanin 16 timing value = 0.0 for cell sc1p3 at line 102
WhatDelayType: Warning! Unknown delay type sc1p8 at line 102 for ce
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Warning! sc1p8 latch fanin 16 timing value = 0.0 for cell sc1p3 at line 102
WhatDelayType: Warning! Unknown delay type sc1p8 at line 102 for ce
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Warning! sc1p8 flipflop fanin 16 timing value = 0.0 for cell sc1p3 at line 102
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Warning! sc1p8 latchlatch fanin 16 timing value = 0.0 for cell sc1p3 at line 102
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Warning! sc1p8 hrflop fanin 16 timing value = 0.0 for cell sc1p3 at line 102
WhatDelayType: Warning! Unknown delay type sc1p8 at line 102 for ce
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Warning! sc1p8 gate fanin 17 timing value = 0.0 for cell sc1p3 at line 102
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Warning! sc1p8 latch fanin 17 timing value = 0.0 for cell sc1p3 at line 102
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Warning! sc1p8 flipflop fanin 17 timing value = 0.0 for cell sc1p3 at line 102
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Warning! sc1p8 latchlatch fanin 17 timing value = 0.0 for cell sc1p3 at line 102
WhatDelayType: Warning! Unknown delay type sc1p8 at line 102 for ce
ll sc1p3

Warning! sc1p8 hrflop fanin 17 timing value = 0.0 for cell sc1p3 at line 102
WhatDelayType: Warning! Unknown delay type sc2p3 at line 107 for ce
ll sc1p3

Warning! sc2p3 gate fanin 1 timing value = 0.0 for cell sc1p3 at line 107
WhatDelayType: Warning! Unknown delay type sc2p3 at line 107 for ce
ll sc1p3

Warning! sc2p3 latch fanin 1 timing value = 0.0 for cell sc1p3 at line 107
WhatDelayType: Warning! Unknown delay type sc2p3 at line 107 for ce
ll sc1p3

Warning! sc2p3 flipflop fanin 1 timing value = 0.0 for cell sc1p3 at line 107
WhatDelayType: Warning! Unknown delay type sc2p3 at line 107 for ce
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Warning! sc2p3 latchlatch fanin 1 timing value = 0.0 for cell sc1p3 at line 107
WhatDelayType: Warning! Unknown delay type sc2p3 at line 107 for ce
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Warning! sc2p3 hrflop fanin 1 timing value = 0.0 for cell sc1p3 at line 107
WhatDelayType: Warning! Unknown delay type sc2p3 at line 107 for ce
ll sc1p3

Warning! sc2p3 gate fanin 2 timing value = 0.0 for cell sc1p3 at line 107

WhatDelayType: Warning! Unknown delay type sc2p3 at line 107 for ce
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Warning! sc2p3 latch fanin 2 timing value = 0.0 for cell sc1p3 at line 107
WhatDelayType: Warning! Unknown delay type sc2p3 at line 107 for ce
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Warning! sc2p3 flipflop fanin 2 timing value = 0.0 for cell sc1p3 at line 107
WhatDelayType: Warning! Unknown delay type sc2p3 at line 107 for ce
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Warning! sc2p3 latchlatch fanin 2 timing value = 0.0 for cell sc1p3 at line 107
WhatDelayType: Warning! Unknown delay type sc2p3 at line 107 for ce
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Warning! sc2p3 hrflop fanin 2 timing value = 0.0 for cell sc1p3 at line 107
WhatDelayType: Warning! Unknown delay type sc2p3 at line 107 for ce
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Warning! sc2p3 gate fanin 3 timing value = 0.0 for cell sc1p3 at line 107
WhatDelayType: Warning! Unknown delay type sc2p3 at line 107 for ce
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Warning! sc2p3 latch fanin 3 timing value = 0.0 for cell sc1p3 at line 107
WhatDelayType: Warning! Unknown delay type sc2p3 at line 107 for ce
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Warning! sc2p3 flipflop fanin 3 timing value = 0.0 for cell sc1p3 at line 107
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Warning! sc2p3 latchlatch fanin 3 timing value = 0.0 for cell sc1p3 at line 107
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Warning! sc2p3 hrflop fanin 3 timing value = 0.0 for cell sc1p3 at line 107
WhatDelayType: Warning! Unknown delay type sc2p3 at line 107 for ce
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Warning! sc2p3 gate fanin 4 timing value = 0.0 for cell sc1p3 at line 107
WhatDelayType: Warning! Unknown delay type sc2p3 at line 107 for ce
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Warning! sc2p3 latch fanin 4 timing value = 0.0 for cell sc1p3 at line 107
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Warning! sc2p3 flipflop fanin 4 timing value = 0.0 for cell sc1p3 at line 107
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Warning! sc2p3 latchlatch fanin 4 timing value = 0.0 for cell sc1p3 at line 107
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Warning! sc2p3 hrflop fanin 4 timing value = 0.0 for cell sc1p3 at line 107
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Warning! sc2p3 gate fanin 5 timing value = 0.0 for cell sc1p3 at line 107
WhatDelayType: Warning! Unknown delay type sc2p3 at line 107 for ce

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Warning! sc2p3 latch fanin 5 timing value = 0.0 for cell sc1p3 at line 107
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Warning! sc2p3 flipflop fanin 5 timing value = 0.0 for cell sc1p3 at line 107
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Warning! sc2p3 latchlatch fanin 5 timing value = 0.0 for cell sc1p3 at line 107
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Warning! sc2p3 hrflop fanin 5 timing value = 0.0 for cell sc1p3 at line 107
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Warning! sc2p3 gate fanin 6 timing value = 0.0 for cell sc1p3 at line 107
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Warning! sc2p3 latch fanin 6 timing value = 0.0 for cell sc1p3 at line 107
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Warning! sc2p3 flipflop fanin 6 timing value = 0.0 for cell sc1p3 at line 107
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Warning! sc2p3 latchlatch fanin 6 timing value = 0.0 for cell sc1p3 at line 107
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Warning! sc2p3 hrflop fanin 6 timing value = 0.0 for cell sc1p3 at line 107
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Warning! sc2p3 gate fanin 7 timing value = 0.0 for cell sc1p3 at line 107
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Warning! sc2p3 latch fanin 7 timing value = 0.0 for cell sc1p3 at line 107
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Warning! sc2p3 flipflop fanin 7 timing value = 0.0 for cell sc1p3 at line 107
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Warning! sc2p3 latchlatch fanin 7 timing value = 0.0 for cell sc1p3 at line 107
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Warning! sc2p3 hrflop fanin 7 timing value = 0.0 for cell sc1p3 at line 107
WhatDelayType: Warning! Unknown delay type sc2p3 at line 107 for ce
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Warning! sc2p3 gate fanin 8 timing value = 0.0 for cell sc1p3 at line 107
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Warning! sc2p3 latch fanin 8 timing value = 0.0 for cell sc1p3 at line 107
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Warning! sc2p3 flipflop fanin 8 timing value = 0.0 for cell sc1p3 at line 107
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Warning! sc2p3 latchlatch fanin 8 timing value = 0.0 for cell sc1p3 at line 107
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Warning! sc2p3 hrflop fanin 8 timing value = 0.0 for cell sc1p3 at line 107
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Warning! sc2p3 gate fanin 9 timing value = 0.0 for cell sc1p3 at line 107
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Warning! sc2p3 latch fanin 9 timing value = 0.0 for cell sc1p3 at line 107
WhatDelayType: Warning! Unknown delay type sc2p3 at line 107 for ce
ll sc1p3

Warning! sc2p3 flipflop fanin 9 timing value = 0.0 for cell sc1p3 at line 107
WhatDelayType: Warning! Unknown delay type sc2p3 at line 107 for ce
ll sc1p3

Warning! sc2p3 latchlatch fanin 9 timing value = 0.0 for cell sc1p3 at line 107
WhatDelayType: Warning! Unknown delay type sc2p3 at line 107 for ce
ll sc1p3

Warning! sc2p3 hrflop fanin 9 timing value = 0.0 for cell sc1p3 at line 107
WhatDelayType: Warning! Unknown delay type sc2p3 at line 107 for ce
ll sc1p3

Warning! sc2p3 gate fanin 10 timing value = 0.0 for cell sc1p3 at line 107
WhatDelayType: Warning! Unknown delay type sc2p3 at line 107 for ce
ll sc1p3

Warning! sc2p3 latch fanin 10 timing value = 0.0 for cell sc1p3 at line 107
WhatDelayType: Warning! Unknown delay type sc2p3 at line 107 for ce
ll sc1p3

Warning! sc2p3 flipflop fanin 10 timing value = 0.0 for cell sc1p3 at line 107
WhatDelayType: Warning! Unknown delay type sc2p3 at line 107 for ce
ll sc1p3

Warning! sc2p3 latchlatch fanin 10 timing value = 0.0 for cell sc1p3 at line 107
WhatDelayType: Warning! Unknown delay type sc2p3 at line 107 for ce
ll sc1p3

Warning! sc2p3 hrflop fanin 10 timing value = 0.0 for cell sc1p3 at line 107
WhatDelayType: Warning! Unknown delay type sc2p3 at line 107 for ce
ll sc1p3

Warning! sc2p3 gate fanin 11 timing value = 0.0 for cell sc1p3 at line 107
WhatDelayType: Warning! Unknown delay type sc2p3 at line 107 for ce
ll sc1p3

Warning! sc2p3 latch fanin 11 timing value = 0.0 for cell sc1p3 at line 107
WhatDelayType: Warning! Unknown delay type sc2p3 at line 107 for ce
ll sc1p3

Warning! sc2p3 flipflop fanin 11 timing value = 0.0 for cell sc1p3 at line 107
WhatDelayType: Warning! Unknown delay type sc2p3 at line 107 for ce
ll sc1p3

Warning! sc2p3 latchlatch fanin 11 timing value = 0.0 for cell sc1p3 at line 107
WhatDelayType: Warning! Unknown delay type sc2p3 at line 107 for ce
ll sc1p3

Warning! sc2p3 hrflop fanin 11 timing value = 0.0 for cell sc1p3 at line 107
WhatDelayType: Warning! Unknown delay type sc2p3 at line 107 for ce
ll sc1p3

Warning! sc2p3 gate fanin 12 timing value = 0.0 for cell sc1p3 at line 107
WhatDelayType: Warning! Unknown delay type sc2p3 at line 107 for ce
ll sc1p3

Warning! sc2p3 latch fanin 12 timing value = 0.0 for cell sc1p3 at line 107
WhatDelayType: Warning! Unknown delay type sc2p3 at line 107 for ce
ll sc1p3

Warning! sc2p3 flipflop fanin 12 timing value = 0.0 for cell sc1p3 at line 107
WhatDelayType: Warning! Unknown delay type sc2p3 at line 107 for ce
ll sc1p3

Warning! sc2p3 latchlatch fanin 12 timing value = 0.0 for cell sc1p3 at line 107
WhatDelayType: Warning! Unknown delay type sc2p3 at line 107 for ce
ll sc1p3

Warning! sc2p3 hrflop fanin 12 timing value = 0.0 for cell sc1p3 at line 107
WhatDelayType: Warning! Unknown delay type sc2p3 at line 107 for ce
ll sc1p3

Warning! sc2p3 gate fanin 13 timing value = 0.0 for cell sc1p3 at line 107
WhatDelayType: Warning! Unknown delay type sc2p3 at line 107 for ce
ll sc1p3

Warning! sc2p3 latch fanin 13 timing value = 0.0 for cell sc1p3 at line 107
WhatDelayType: Warning! Unknown delay type sc2p3 at line 107 for ce
ll sc1p3

Warning! sc2p3 flipflop fanin 13 timing value = 0.0 for cell sc1p3 at line 107
WhatDelayType: Warning! Unknown delay type sc2p3 at line 107 for ce
ll sc1p3

Warning! sc2p3 latchlatch fanin 13 timing value = 0.0 for cell sc1p3 at line 107
WhatDelayType: Warning! Unknown delay type sc2p3 at line 107 for ce
ll sc1p3

Warning! sc2p3 hrflop fanin 13 timing value = 0.0 for cell sc1p3 at line 107
WhatDelayType: Warning! Unknown delay type sc2p3 at line 107 for ce
ll sc1p3

Warning! sc2p3 gate fanin 14 timing value = 0.0 for cell sc1p3 at line 107
WhatDelayType: Warning! Unknown delay type sc2p3 at line 107 for ce
ll sc1p3

Warning! sc2p3 latch fanin 14 timing value = 0.0 for cell sc1p3 at line 107

WhatDelayType: Warning! Unknown delay type sc2p3 at line 107 for ce
ll sc1p3

Warning! sc2p3 flipflop fanin 14 timing value = 0.0 for cell sc1p3 at line 107
WhatDelayType: Warning! Unknown delay type sc2p3 at line 107 for ce
ll sc1p3

Warning! sc2p3 latchlatch fanin 14 timing value = 0.0 for cell sc1p3 at line 107
WhatDelayType: Warning! Unknown delay type sc2p3 at line 107 for ce
ll sc1p3

Warning! sc2p3 hrflop fanin 14 timing value = 0.0 for cell sc1p3 at line 107
WhatDelayType: Warning! Unknown delay type sc2p3 at line 107 for ce
ll sc1p3

Warning! sc2p3 gate fanin 15 timing value = 0.0 for cell sc1p3 at line 107
WhatDelayType: Warning! Unknown delay type sc2p3 at line 107 for ce
ll sc1p3

Warning! sc2p3 latch fanin 15 timing value = 0.0 for cell sc1p3 at line 107
WhatDelayType: Warning! Unknown delay type sc2p3 at line 107 for ce
ll sc1p3

Warning! sc2p3 flipflop fanin 15 timing value = 0.0 for cell sc1p3 at line 107
WhatDelayType: Warning! Unknown delay type sc2p3 at line 107 for ce
ll sc1p3

Warning! sc2p3 latchlatch fanin 15 timing value = 0.0 for cell sc1p3 at line 107
WhatDelayType: Warning! Unknown delay type sc2p3 at line 107 for ce
ll sc1p3

Warning! sc2p3 hrflop fanin 15 timing value = 0.0 for cell sc1p3 at line 107
WhatDelayType: Warning! Unknown delay type sc2p3 at line 107 for ce
ll sc1p3

Warning! sc2p3 gate fanin 16 timing value = 0.0 for cell sc1p3 at line 107
WhatDelayType: Warning! Unknown delay type sc2p3 at line 107 for ce
ll sc1p3

Warning! sc2p3 latch fanin 16 timing value = 0.0 for cell sc1p3 at line 107
WhatDelayType: Warning! Unknown delay type sc2p3 at line 107 for ce
ll sc1p3

Warning! sc2p3 flipflop fanin 16 timing value = 0.0 for cell sc1p3 at line 107
WhatDelayType: Warning! Unknown delay type sc2p3 at line 107 for ce
ll sc1p3

Warning! sc2p3 latchlatch fanin 16 timing value = 0.0 for cell sc1p3 at line 107
WhatDelayType: Warning! Unknown delay type sc2p3 at line 107 for ce
ll sc1p3

Warning! sc2p3 hrflop fanin 16 timing value = 0.0 for cell sc1p3 at line 107
WhatDelayType: Warning! Unknown delay type sc2p3 at line 107 for ce
ll sc1p3

Warning! sc2p3 gate fanin 17 timing value = 0.0 for cell sc1p3 at line 107
WhatDelayType: Warning! Unknown delay type sc2p3 at line 107 for ce
ll sc1p3

Warning! sc2p3 latch fanin 17 timing value = 0.0 for cell sc1p3 at line 107
WhatDelayType: Warning! Unknown delay type sc2p3 at line 107 for ce

ll sc1p3

Warning! sc2p3 flipflop fanin 17 timing value = 0.0 for cell sc1p3 at line 107
WhatDelayType: Warning! Unknown delay type sc2p3 at line 107 for ce
ll sc1p3

Warning! sc2p3 latchlatch fanin 17 timing value = 0.0 for cell sc1p3 at line 107
WhatDelayType: Warning! Unknown delay type sc2p3 at line 107 for ce
ll sc1p3

Warning! sc2p3 hrflop fanin 17 timing value = 0.0 for cell sc1p3 at line 107
WhatDelayType: Warning! Unknown delay type sc2p8 at line 112 for ce
ll sc1p3

Warning! sc2p8 gate fanin 1 timing value = 0.0 for cell sc1p3 at line 112
WhatDelayType: Warning! Unknown delay type sc2p8 at line 112 for ce
ll sc1p3

Warning! sc2p8 latch fanin 1 timing value = 0.0 for cell sc1p3 at line 112
WhatDelayType: Warning! Unknown delay type sc2p8 at line 112 for ce
ll sc1p3

Warning! sc2p8 flipflop fanin 1 timing value = 0.0 for cell sc1p3 at line 112
WhatDelayType: Warning! Unknown delay type sc2p8 at line 112 for ce
ll sc1p3

Warning! sc2p8 latchlatch fanin 1 timing value = 0.0 for cell sc1p3 at line 112
WhatDelayType: Warning! Unknown delay type sc2p8 at line 112 for ce
ll sc1p3

Warning! sc2p8 hrflop fanin 1 timing value = 0.0 for cell sc1p3 at line 112
WhatDelayType: Warning! Unknown delay type sc2p8 at line 112 for ce
ll sc1p3

Warning! sc2p8 gate fanin 2 timing value = 0.0 for cell sc1p3 at line 112
WhatDelayType: Warning! Unknown delay type sc2p8 at line 112 for ce
ll sc1p3

Warning! sc2p8 latch fanin 2 timing value = 0.0 for cell sc1p3 at line 112
WhatDelayType: Warning! Unknown delay type sc2p8 at line 112 for ce
ll sc1p3

Warning! sc2p8 flipflop fanin 2 timing value = 0.0 for cell sc1p3 at line 112
WhatDelayType: Warning! Unknown delay type sc2p8 at line 112 for ce
ll sc1p3

Warning! sc2p8 latchlatch fanin 2 timing value = 0.0 for cell sc1p3 at line 112
WhatDelayType: Warning! Unknown delay type sc2p8 at line 112 for ce
ll sc1p3

Warning! sc2p8 hrflop fanin 2 timing value = 0.0 for cell sc1p3 at line 112
WhatDelayType: Warning! Unknown delay type sc2p8 at line 112 for ce
ll sc1p3

Warning! sc2p8 gate fanin 3 timing value = 0.0 for cell sc1p3 at line 112
WhatDelayType: Warning! Unknown delay type sc2p8 at line 112 for ce
ll sc1p3

Warning! sc2p8 latch fanin 3 timing value = 0.0 for cell sc1p3 at line 112
WhatDelayType: Warning! Unknown delay type sc2p8 at line 112 for ce
ll sc1p3

Warning! sc2p8 flipflop fanin 3 timing value = 0.0 for cell sc1p3 at line 112
WhatDelayType: Warning! Unknown delay type sc2p8 at line 112 for ce
ll sc1p3

Warning! sc2p8 latchlatch fanin 3 timing value = 0.0 for cell sc1p3 at line 112
WhatDelayType: Warning! Unknown delay type sc2p8 at line 112 for ce
ll sc1p3

Warning! sc2p8 hrflop fanin 3 timing value = 0.0 for cell sc1p3 at line 112
WhatDelayType: Warning! Unknown delay type sc2p8 at line 112 for ce
ll sc1p3

Warning! sc2p8 gate fanin 4 timing value = 0.0 for cell sc1p3 at line 112
WhatDelayType: Warning! Unknown delay type sc2p8 at line 112 for ce
ll sc1p3

Warning! sc2p8 latch fanin 4 timing value = 0.0 for cell sc1p3 at line 112
WhatDelayType: Warning! Unknown delay type sc2p8 at line 112 for ce
ll sc1p3

Warning! sc2p8 flipflop fanin 4 timing value = 0.0 for cell sc1p3 at line 112
WhatDelayType: Warning! Unknown delay type sc2p8 at line 112 for ce
ll sc1p3

Warning! sc2p8 latchlatch fanin 4 timing value = 0.0 for cell sc1p3 at line 112
WhatDelayType: Warning! Unknown delay type sc2p8 at line 112 for ce
ll sc1p3

Warning! sc2p8 hrflop fanin 4 timing value = 0.0 for cell sc1p3 at line 112
WhatDelayType: Warning! Unknown delay type sc2p8 at line 112 for ce
ll sc1p3

Warning! sc2p8 gate fanin 5 timing value = 0.0 for cell sc1p3 at line 112
WhatDelayType: Warning! Unknown delay type sc2p8 at line 112 for ce
ll sc1p3

Warning! sc2p8 latch fanin 5 timing value = 0.0 for cell sc1p3 at line 112
WhatDelayType: Warning! Unknown delay type sc2p8 at line 112 for ce
ll sc1p3

Warning! sc2p8 flipflop fanin 5 timing value = 0.0 for cell sc1p3 at line 112
WhatDelayType: Warning! Unknown delay type sc2p8 at line 112 for ce
ll sc1p3

Warning! sc2p8 latchlatch fanin 5 timing value = 0.0 for cell sc1p3 at line 112
WhatDelayType: Warning! Unknown delay type sc2p8 at line 112 for ce
ll sc1p3

Warning! sc2p8 hrflop fanin 5 timing value = 0.0 for cell sc1p3 at line 112
WhatDelayType: Warning! Unknown delay type sc2p8 at line 112 for ce
ll sc1p3

Warning! sc2p8 gate fanin 6 timing value = 0.0 for cell sc1p3 at line 112
WhatDelayType: Warning! Unknown delay type sc2p8 at line 112 for ce
ll sc1p3

Warning! sc2p8 latch fanin 6 timing value = 0.0 for cell sc1p3 at line 112
WhatDelayType: Warning! Unknown delay type sc2p8 at line 112 for ce
ll sc1p3

Warning! sc2p8 flipflop fanin 6 timing value = 0.0 for cell sc1p3 at line 112
WhatDelayType: Warning! Unknown delay type sc2p8 at line 112 for ce
ll sc1p3

Warning! sc2p8 latchlatch fanin 6 timing value = 0.0 for cell sc1p3 at line 112
WhatDelayType: Warning! Unknown delay type sc2p8 at line 112 for ce
ll sc1p3

Warning! sc2p8 hrflop fanin 6 timing value = 0.0 for cell sc1p3 at line 112
WhatDelayType: Warning! Unknown delay type sc2p8 at line 112 for ce
ll sc1p3

Warning! sc2p8 gate fanin 7 timing value = 0.0 for cell sc1p3 at line 112
WhatDelayType: Warning! Unknown delay type sc2p8 at line 112 for ce
ll sc1p3

Warning! sc2p8 latch fanin 7 timing value = 0.0 for cell sc1p3 at line 112
WhatDelayType: Warning! Unknown delay type sc2p8 at line 112 for ce
ll sc1p3

Warning! sc2p8 flipflop fanin 7 timing value = 0.0 for cell sc1p3 at line 112
WhatDelayType: Warning! Unknown delay type sc2p8 at line 112 for ce
ll sc1p3

Warning! sc2p8 latchlatch fanin 7 timing value = 0.0 for cell sc1p3 at line 112
WhatDelayType: Warning! Unknown delay type sc2p8 at line 112 for ce
ll sc1p3

Warning! sc2p8 hrflop fanin 7 timing value = 0.0 for cell sc1p3 at line 112
WhatDelayType: Warning! Unknown delay type sc2p8 at line 112 for ce
ll sc1p3

Warning! sc2p8 gate fanin 8 timing value = 0.0 for cell sc1p3 at line 112
WhatDelayType: Warning! Unknown delay type sc2p8 at line 112 for ce
ll sc1p3

Warning! sc2p8 latch fanin 8 timing value = 0.0 for cell sc1p3 at line 112
WhatDelayType: Warning! Unknown delay type sc2p8 at line 112 for ce
ll sc1p3

Warning! sc2p8 flipflop fanin 8 timing value = 0.0 for cell sc1p3 at line 112
WhatDelayType: Warning! Unknown delay type sc2p8 at line 112 for ce
ll sc1p3

Warning! sc2p8 latchlatch fanin 8 timing value = 0.0 for cell sc1p3 at line 112
WhatDelayType: Warning! Unknown delay type sc2p8 at line 112 for ce
ll sc1p3

Warning! sc2p8 hrflop fanin 8 timing value = 0.0 for cell sc1p3 at line 112
WhatDelayType: Warning! Unknown delay type sc2p8 at line 112 for ce
ll sc1p3

Warning! sc2p8 gate fanin 9 timing value = 0.0 for cell sc1p3 at line 112
WhatDelayType: Warning! Unknown delay type sc2p8 at line 112 for ce
ll sc1p3

Warning! sc2p8 latch fanin 9 timing value = 0.0 for cell sc1p3 at line 112
WhatDelayType: Warning! Unknown delay type sc2p8 at line 112 for ce
ll sc1p3

Warning! sc2p8 flipflop fanin 9 timing value = 0.0 for cell sc1p3 at line 112

WhatDelayType: Warning! Unknown delay type sc2p8 at line 112 for ce
ll sc1p3

Warning! sc2p8 latchlatch fanin 9 timing value = 0.0 for cell sc1p3 at line 112
WhatDelayType: Warning! Unknown delay type sc2p8 at line 112 for ce
ll sc1p3

Warning! sc2p8 hrflop fanin 9 timing value = 0.0 for cell sc1p3 at line 112
WhatDelayType: Warning! Unknown delay type sc2p8 at line 112 for ce
ll sc1p3

Warning! sc2p8 gate fanin 10 timing value = 0.0 for cell sc1p3 at line 112
WhatDelayType: Warning! Unknown delay type sc2p8 at line 112 for ce
ll sc1p3

Warning! sc2p8 latch fanin 10 timing value = 0.0 for cell sc1p3 at line 112
WhatDelayType: Warning! Unknown delay type sc2p8 at line 112 for ce
ll sc1p3

Warning! sc2p8 flipflop fanin 10 timing value = 0.0 for cell sc1p3 at line 112
WhatDelayType: Warning! Unknown delay type sc2p8 at line 112 for ce
ll sc1p3

Warning! sc2p8 latchlatch fanin 10 timing value = 0.0 for cell sc1p3 at line 112
WhatDelayType: Warning! Unknown delay type sc2p8 at line 112 for ce
ll sc1p3

Warning! sc2p8 hrflop fanin 10 timing value = 0.0 for cell sc1p3 at line 112
WhatDelayType: Warning! Unknown delay type sc2p8 at line 112 for ce
ll sc1p3

Warning! sc2p8 gate fanin 11 timing value = 0.0 for cell sc1p3 at line 112
WhatDelayType: Warning! Unknown delay type sc2p8 at line 112 for ce
ll sc1p3

Warning! sc2p8 latch fanin 11 timing value = 0.0 for cell sc1p3 at line 112
WhatDelayType: Warning! Unknown delay type sc2p8 at line 112 for ce
ll sc1p3

Warning! sc2p8 flipflop fanin 11 timing value = 0.0 for cell sc1p3 at line 112
WhatDelayType: Warning! Unknown delay type sc2p8 at line 112 for ce
ll sc1p3

Warning! sc2p8 latchlatch fanin 11 timing value = 0.0 for cell sc1p3 at line 112
WhatDelayType: Warning! Unknown delay type sc2p8 at line 112 for ce
ll sc1p3

Warning! sc2p8 hrflop fanin 11 timing value = 0.0 for cell sc1p3 at line 112
WhatDelayType: Warning! Unknown delay type sc2p8 at line 112 for ce
ll sc1p3

Warning! sc2p8 gate fanin 12 timing value = 0.0 for cell sc1p3 at line 112
WhatDelayType: Warning! Unknown delay type sc2p8 at line 112 for ce
ll sc1p3

Warning! sc2p8 latch fanin 12 timing value = 0.0 for cell sc1p3 at line 112
WhatDelayType: Warning! Unknown delay type sc2p8 at line 112 for ce
ll sc1p3

Warning! sc2p8 flipflop fanin 12 timing value = 0.0 for cell sc1p3 at line 112
WhatDelayType: Warning! Unknown delay type sc2p8 at line 112 for ce

ll sc1p3

Warning! sc2p8 latchlatch fanin 12 timing value = 0.0 for cell sc1p3 at line 112
WhatDelayType: Warning! Unknown delay type sc2p8 at line 112 for ce
ll sc1p3

Warning! sc2p8 hrflop fanin 12 timing value = 0.0 for cell sc1p3 at line 112
WhatDelayType: Warning! Unknown delay type sc2p8 at line 112 for ce
ll sc1p3

Warning! sc2p8 gate fanin 13 timing value = 0.0 for cell sc1p3 at line 112
WhatDelayType: Warning! Unknown delay type sc2p8 at line 112 for ce
ll sc1p3

Warning! sc2p8 latch fanin 13 timing value = 0.0 for cell sc1p3 at line 112
WhatDelayType: Warning! Unknown delay type sc2p8 at line 112 for ce
ll sc1p3

Warning! sc2p8 flipflop fanin 13 timing value = 0.0 for cell sc1p3 at line 112
WhatDelayType: Warning! Unknown delay type sc2p8 at line 112 for ce
ll sc1p3

Warning! sc2p8 latchlatch fanin 13 timing value = 0.0 for cell sc1p3 at line 112
WhatDelayType: Warning! Unknown delay type sc2p8 at line 112 for ce
ll sc1p3

Warning! sc2p8 hrflop fanin 13 timing value = 0.0 for cell sc1p3 at line 112
WhatDelayType: Warning! Unknown delay type sc2p8 at line 112 for ce
ll sc1p3

Warning! sc2p8 gate fanin 14 timing value = 0.0 for cell sc1p3 at line 112
WhatDelayType: Warning! Unknown delay type sc2p8 at line 112 for ce
ll sc1p3

Warning! sc2p8 latch fanin 14 timing value = 0.0 for cell sc1p3 at line 112
WhatDelayType: Warning! Unknown delay type sc2p8 at line 112 for ce
ll sc1p3

Warning! sc2p8 flipflop fanin 14 timing value = 0.0 for cell sc1p3 at line 112
WhatDelayType: Warning! Unknown delay type sc2p8 at line 112 for ce
ll sc1p3

Warning! sc2p8 latchlatch fanin 14 timing value = 0.0 for cell sc1p3 at line 112
WhatDelayType: Warning! Unknown delay type sc2p8 at line 112 for ce
ll sc1p3

Warning! sc2p8 hrflop fanin 14 timing value = 0.0 for cell sc1p3 at line 112
WhatDelayType: Warning! Unknown delay type sc2p8 at line 112 for ce
ll sc1p3

Warning! sc2p8 gate fanin 15 timing value = 0.0 for cell sc1p3 at line 112
WhatDelayType: Warning! Unknown delay type sc2p8 at line 112 for ce
ll sc1p3

Warning! sc2p8 latch fanin 15 timing value = 0.0 for cell sc1p3 at line 112
WhatDelayType: Warning! Unknown delay type sc2p8 at line 112 for ce
ll sc1p3

Warning! sc2p8 flipflop fanin 15 timing value = 0.0 for cell sc1p3 at line 112
WhatDelayType: Warning! Unknown delay type sc2p8 at line 112 for ce
ll sc1p3

Warning! sc2p8 latchlatch fanin 15 timing value = 0.0 for cell sc1p3 at line 112
WhatDelayType: Warning! Unknown delay type sc2p8 at line 112 for ce
ll sc1p3

Warning! sc2p8 hrflop fanin 15 timing value = 0.0 for cell sc1p3 at line 112
WhatDelayType: Warning! Unknown delay type sc2p8 at line 112 for ce
ll sc1p3

Warning! sc2p8 gate fanin 16 timing value = 0.0 for cell sc1p3 at line 112
WhatDelayType: Warning! Unknown delay type sc2p8 at line 112 for ce
ll sc1p3

Warning! sc2p8 latch fanin 16 timing value = 0.0 for cell sc1p3 at line 112
WhatDelayType: Warning! Unknown delay type sc2p8 at line 112 for ce
ll sc1p3

Warning! sc2p8 flipflop fanin 16 timing value = 0.0 for cell sc1p3 at line 112
WhatDelayType: Warning! Unknown delay type sc2p8 at line 112 for ce
ll sc1p3

Warning! sc2p8 latchlatch fanin 16 timing value = 0.0 for cell sc1p3 at line 112
WhatDelayType: Warning! Unknown delay type sc2p8 at line 112 for ce
ll sc1p3

Warning! sc2p8 hrflop fanin 16 timing value = 0.0 for cell sc1p3 at line 112
WhatDelayType: Warning! Unknown delay type sc2p8 at line 112 for ce
ll sc1p3

Warning! sc2p8 gate fanin 17 timing value = 0.0 for cell sc1p3 at line 112
WhatDelayType: Warning! Unknown delay type sc2p8 at line 112 for ce
ll sc1p3

Warning! sc2p8 latch fanin 17 timing value = 0.0 for cell sc1p3 at line 112
WhatDelayType: Warning! Unknown delay type sc2p8 at line 112 for ce
ll sc1p3

Warning! sc2p8 flipflop fanin 17 timing value = 0.0 for cell sc1p3 at line 112
WhatDelayType: Warning! Unknown delay type sc2p8 at line 112 for ce
ll sc1p3

Warning! sc2p8 latchlatch fanin 17 timing value = 0.0 for cell sc1p3 at line 112
WhatDelayType: Warning! Unknown delay type sc2p8 at line 112 for ce
ll sc1p3

Warning! sc2p8 hrflop fanin 17 timing value = 0.0 for cell sc1p3 at line 112 Reading pin cap values
from /n/auspex/s15/tbr/euterpe/proteus/leafgen/caps/cap.lib

From: Tim B. Robinson [tbr@aphrodite]
Sent: Friday, September 16, 1994 11:04 AM
To: 'geert@aphrodite'; 'hopper@aphrodite'
Cc: 'vanthof@aphrodite'
Subject: Bogus data

This lot came back in one of my runs last night:

WhatDelayType: Warning! Unknown delay type iobyte at line 62 for ce
ll iobyte

Warning! iobyte gate fanin 1 timing value = 0.0 for cell iobyte at line 62
WhatDelayType: Warning! Unknown delay type iobyte at line 62 for ce
ll iobyte

Warning! iobyte latch fanin 1 timing value = 0.0 for cell iobyte at line
62
WhatDelayType: Warning! Unknown delay type iobyte at line 62 for ce
ll iobyte

Warning! iobyte flipflop fanin 1 timing value = 0.0 for cell iobyte at
line 62
WhatDelayType: Warning! Unknown delay type iobyte at line 62 for ce
ll iobyte

Warning! iobyte latchlatch fanin 1 timing value = 0.0 for cell iobyte at
line 62
WhatDelayType: Warning! Unknown delay type iobyte at line 62 for ce
ll iobyte

Warning! iobyte hrflop fanin 1 timing value = 0.0 for cell iobyte at line
62
WhatDelayType: Warning! Unknown delay type iobyte at line 62 for ce
ll iobyte

Warning! iobyte gate fanin 2 timing value = 0.0 for cell iobyte at line 62
WhatDelayType: Warning! Unknown delay type iobyte at line 62 for ce
ll iobyte

Warning! iobyte latch fanin 2 timing value = 0.0 for cell iobyte at line
62
WhatDelayType: Warning! Unknown delay type iobyte at line 62 for ce
ll iobyte

Warning! iobyte flipflop fanin 2 timing value = 0.0 for cell iobyte at
line 62
WhatDelayType: Warning! Unknown delay type iobyte at line 62 for ce
ll iobyte

Warning! iobyte latchlatch fanin 2 timing value = 0.0 for cell iobyte at
line 62
WhatDelayType: Warning! Unknown delay type iobyte at line 62 for ce
ll iobyte

Warning! iobyte hrflop fanin 2 timing value = 0.0 for cell iobyte at line
62
WhatDelayType: Warning! Unknown delay type iobyte at line 62 for ce
ll iobyte

Warning! iobyte gate fanin 3 timing value = 0.0 for cell iobyte at line 62
WhatDelayType: Warning! Unknown delay type iobyte at line 62 for ce
ll iobyte

Warning! iobyte latch fanin 3 timing value = 0.0 for cell iobyte at line 62
WhatDelayType: Warning! Unknown delay type iobyte at line 62 for ce ll iobyte

Warning! iobyte flipflop fanin 3 timing value = 0.0 for cell iobyte at line 62
WhatDelayType: Warning! Unknown delay type iobyte at line 62 for ce ll iobyte

Warning! iobyte latchlatch fanin 3 timing value = 0.0 for cell iobyte at line 62
WhatDelayType: Warning! Unknown delay type iobyte at line 62 for ce ll iobyte

Warning! iobyte hrflop fanin 3 timing value = 0.0 for cell iobyte at line 62
WhatDelayType: Warning! Unknown delay type iobyte at line 62 for ce ll iobyte

Warning! iobyte gate fanin 4 timing value = 0.0 for cell iobyte at line 62
WhatDelayType: Warning! Unknown delay type iobyte at line 62 for ce ll iobyte

Warning! iobyte latch fanin 4 timing value = 0.0 for cell iobyte at line 62
WhatDelayType: Warning! Unknown delay type iobyte at line 62 for ce ll iobyte

Warning! iobyte flipflop fanin 4 timing value = 0.0 for cell iobyte at line 62
WhatDelayType: Warning! Unknown delay type iobyte at line 62 for ce ll iobyte

Warning! iobyte latchlatch fanin 4 timing value = 0.0 for cell iobyte at line 62
WhatDelayType: Warning! Unknown delay type iobyte at line 62 for ce ll iobyte

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Warning! sc1p3 hrflop fanin 1 timing value = 0.0 for cell sc1p3 at line 97

WhatDelayType: Warning! Unknown delay type sc1p3 at line 97 for ce
ll sc1p3

Warning! sc1p3 gate fanin 2 timing value = 0.0 for cell sc1p3 at line 97

WhatDelayType: Warning! Unknown delay type sc1p3 at line 97 for ce
ll sc1p3

Warning! sc1p3 latch fanin 2 timing value = 0.0 for cell sc1p3 at line 97

WhatDelayType: Warning! Unknown delay type sc1p3 at line 97 for ce
ll sc1p3

Warning! sc1p3 flipflop fanin 2 timing value = 0.0 for cell sc1p3 at line
97

WhatDelayType: Warning! Unknown delay type sc1p3 at line 97 for ce
ll sc1p3

Warning! sc1p3 latchlatch fanin 2 timing value = 0.0 for cell sc1p3 at line 97
WhatDelayType: Warning! Unknown delay type sc1p3 at line 97 for ce
ll sc1p3

Warning! sc1p3 hrflop fanin 2 timing value = 0.0 for cell sc1p3 at line 97
WhatDelayType: Warning! Unknown delay type sc1p3 at line 97 for ce
ll sc1p3

Warning! sc1p3 gate fanin 3 timing value = 0.0 for cell sc1p3 at line 97
WhatDelayType: Warning! Unknown delay type sc1p3 at line 97 for ce
ll sc1p3

Warning! sc1p3 latch fanin 3 timing value = 0.0 for cell sc1p3 at line 97
WhatDelayType: Warning! Unknown delay type sc1p3 at line 97 for ce
ll sc1p3

Warning! sc1p3 flipflop fanin 3 timing value = 0.0 for cell sc1p3 at line 97
WhatDelayType: Warning! Unknown delay type sc1p3 at line 97 for ce
ll sc1p3

Warning! sc1p3 latchlatch fanin 3 timing value = 0.0 for cell sc1p3 at line 97
WhatDelayType: Warning! Unknown delay type sc1p3 at line 97 for ce
ll sc1p3

Warning! sc1p3 hrflop fanin 3 timing value = 0.0 for cell sc1p3 at line 97
WhatDelayType: Warning! Unknown delay type sc1p3 at line 97 for ce
ll sc1p3

Warning! sc1p3 gate fanin 4 timing value = 0.0 for cell sc1p3 at line 97
WhatDelayType: Warning! Unknown delay type sc1p3 at line 97 for ce
ll sc1p3

Warning! sc1p3 latch fanin 4 timing value = 0.0 for cell sc1p3 at line 97
WhatDelayType: Warning! Unknown delay type sc1p3 at line 97 for ce
ll sc1p3

Warning! sc1p3 flipflop fanin 4 timing value = 0.0 for cell sc1p3 at line 97
WhatDelayType: Warning! Unknown delay type sc1p3 at line 97 for ce
ll sc1p3

Warning! sc1p3 latchlatch fanin 4 timing value = 0.0 for cell sc1p3 at line 97
WhatDelayType: Warning! Unknown delay type sc1p3 at line 97 for ce
ll sc1p3

Warning! sc1p3 hrflop fanin 4 timing value = 0.0 for cell sc1p3 at line 97
WhatDelayType: Warning! Unknown delay type sc1p3 at line 97 for ce
ll sc1p3

Warning! sc1p3 gate fanin 5 timing value = 0.0 for cell sc1p3 at line 97
WhatDelayType: Warning! Unknown delay type sc1p3 at line 97 for ce
ll sc1p3

Warning! sc1p3 latch fanin 5 timing value = 0.0 for cell sc1p3 at line 97
WhatDelayType: Warning! Unknown delay type sc1p3 at line 97 for ce
ll sc1p3

Warning! sc1p3 flipflop fanin 5 timing value = 0.0 for cell sc1p3 at line 97
WhatDelayType: Warning! Unknown delay type sc1p3 at line 97 for ce
ll sc1p3

Warning! sc1p3 latchlatch fanin 5 timing value = 0.0 for cell sc1p3 at line 97

WhatDelayType: Warning! Unknown delay type sc1p3 at line 97 for ce
ll sc1p3

Warning! sc1p3 hrflop fanin 5 timing value = 0.0 for cell sc1p3 at line 97
WhatDelayType: Warning! Unknown delay type sc1p3 at line 97 for ce
ll sc1p3

Warning! sc1p3 gate fanin 6 timing value = 0.0 for cell sc1p3 at line 97
WhatDelayType: Warning! Unknown delay type sc1p3 at line 97 for ce
ll sc1p3

Warning! sc1p3 latch fanin 6 timing value = 0.0 for cell sc1p3 at line 97
WhatDelayType: Warning! Unknown delay type sc1p3 at line 97 for ce
ll sc1p3

Warning! sc1p3 flipflop fanin 6 timing value = 0.0 for cell sc1p3 at line
97
WhatDelayType: Warning! Unknown delay type sc1p3 at line 97 for ce
ll sc1p3

Warning! sc1p3 latchlatch fanin 6 timing value = 0.0 for cell sc1p3 at
line 97
WhatDelayType: Warning! Unknown delay type sc1p3 at line 97 for ce
ll sc1p3

Warning! sc1p3 hrflop fanin 6 timing value = 0.0 for cell sc1p3 at line 97
WhatDelayType: Warning! Unknown delay type sc1p3 at line 97 for ce
ll sc1p3

Warning! sc1p3 gate fanin 7 timing value = 0.0 for cell sc1p3 at line 97
WhatDelayType: Warning! Unknown delay type sc1p3 at line 97 for ce
ll sc1p3

Warning! sc1p3 latch fanin 7 timing value = 0.0 for cell sc1p3 at line 97
WhatDelayType: Warning! Unknown delay type sc1p3 at line 97 for ce
ll sc1p3

Warning! sc1p3 flipflop fanin 7 timing value = 0.0 for cell sc1p3 at line
97
WhatDelayType: Warning! Unknown delay type sc1p3 at line 97 for ce
ll sc1p3

Warning! sc1p3 latchlatch fanin 7 timing value = 0.0 for cell sc1p3 at
line 97
WhatDelayType: Warning! Unknown delay type sc1p3 at line 97 for ce
ll sc1p3

Warning! sc1p3 hrflop fanin 7 timing value = 0.0 for cell sc1p3 at line 97
WhatDelayType: Warning! Unknown delay type sc1p3 at line 97 for ce
ll sc1p3

Warning! sc1p3 gate fanin 8 timing value = 0.0 for cell sc1p3 at line 97
WhatDelayType: Warning! Unknown delay type sc1p3 at line 97 for ce
ll sc1p3

Warning! sc1p3 latch fanin 8 timing value = 0.0 for cell sc1p3 at line 97
WhatDelayType: Warning! Unknown delay type sc1p3 at line 97 for ce
ll sc1p3

Warning! sc1p3 flipflop fanin 8 timing value = 0.0 for cell sc1p3 at line
97
WhatDelayType: Warning! Unknown delay type sc1p3 at line 97 for ce
ll sc1p3

Warning! sc1p3 latchlatch fanin 8 timing value = 0.0 for cell sc1p3 at
line 97
WhatDelayType: Warning! Unknown delay type sc1p3 at line 97 for ce
ll sc1p3

Warning! sc1p3 hrflop fanin 8 timing value = 0.0 for cell sc1p3 at line 97
WhatDelayType: Warning! Unknown delay type sc1p3 at line 97 for ce
ll sc1p3

Warning! sc1p3 gate fanin 9 timing value = 0.0 for cell sc1p3 at line 97
WhatDelayType: Warning! Unknown delay type sc1p3 at line 97 for ce
ll sc1p3

Warning! sc1p3 latch fanin 9 timing value = 0.0 for cell sc1p3 at line 97
WhatDelayType: Warning! Unknown delay type sc1p3 at line 97 for ce
ll sc1p3

Warning! sc1p3 flipflop fanin 9 timing value = 0.0 for cell sc1p3 at line
97
WhatDelayType: Warning! Unknown delay type sc1p3 at line 97 for ce
ll sc1p3

Warning! sc1p3 latchlatch fanin 9 timing value = 0.0 for cell sc1p3 at
line 97
WhatDelayType: Warning! Unknown delay type sc1p3 at line 97 for ce
ll sc1p3

Warning! sc1p3 hrflop fanin 9 timing value = 0.0 for cell sc1p3 at line 97
WhatDelayType: Warning! Unknown delay type sc1p3 at line 97 for ce
ll sc1p3

Warning! sc1p3 gate fanin 10 timing value = 0.0 for cell sc1p3 at line 97
WhatDelayType: Warning! Unknown delay type sc1p3 at line 97 for ce
ll sc1p3

Warning! sc1p3 latch fanin 10 timing value = 0.0 for cell sc1p3 at line 97
WhatDelayType: Warning! Unknown delay type sc1p3 at line 97 for ce
ll sc1p3

Warning! sc1p3 flipflop fanin 10 timing value = 0.0 for cell sc1p3 at line
97
WhatDelayType: Warning! Unknown delay type sc1p3 at line 97 for ce
ll sc1p3

Warning! sc1p3 latchlatch fanin 10 timing value = 0.0 for cell sc1p3 at
line 97
WhatDelayType: Warning! Unknown delay type sc1p3 at line 97 for ce
ll sc1p3

Warning! sc1p3 hrflop fanin 10 timing value = 0.0 for cell sc1p3 at line
97
WhatDelayType: Warning! Unknown delay type sc1p3 at line 97 for ce
ll sc1p3

Warning! sc1p3 gate fanin 11 timing value = 0.0 for cell sc1p3 at line 97
WhatDelayType: Warning! Unknown delay type sc1p3 at line 97 for ce
ll sc1p3

Warning! sc1p3 latch fanin 11 timing value = 0.0 for cell sc1p3 at line 97
WhatDelayType: Warning! Unknown delay type sc1p3 at line 97 for ce
ll sc1p3

Warning! sc1p3 flipflop fanin 11 timing value = 0.0 for cell sc1p3 at line
97
WhatDelayType: Warning! Unknown delay type sc1p3 at line 97 for ce
ll sc1p3

Warning! sc1p3 latchlatch fanin 11 timing value = 0.0 for cell sc1p3 at
line 97
WhatDelayType: Warning! Unknown delay type sc1p3 at line 97 for ce
ll sc1p3

Warning! sc1p3 hrflop fanin 11 timing value = 0.0 for cell sc1p3 at line 97
WhatDelayType: Warning! Unknown delay type sc1p3 at line 97 for ce
11 sc1p3

Warning! sc1p3 gate fanin 12 timing value = 0.0 for cell sc1p3 at line 97
WhatDelayType: Warning! Unknown delay type sc1p3 at line 97 for ce
11 sc1p3

Warning! sc1p3 latch fanin 12 timing value = 0.0 for cell sc1p3 at line 97
WhatDelayType: Warning! Unknown delay type sc1p3 at line 97 for ce
11 sc1p3

Warning! sc1p3 flipflop fanin 12 timing value = 0.0 for cell sc1p3 at line 97
WhatDelayType: Warning! Unknown delay type sc1p3 at line 97 for ce
11 sc1p3

Warning! sc1p3 latchlatch fanin 12 timing value = 0.0 for cell sc1p3 at line 97
WhatDelayType: Warning! Unknown delay type sc1p3 at line 97 for ce
11 sc1p3

Warning! sc1p3 hrflop fanin 12 timing value = 0.0 for cell sc1p3 at line 97
WhatDelayType: Warning! Unknown delay type sc1p3 at line 97 for ce
11 sc1p3

Warning! sc1p3 gate fanin 13 timing value = 0.0 for cell sc1p3 at line 97
WhatDelayType: Warning! Unknown delay type sc1p3 at line 97 for ce
11 sc1p3

Warning! sc1p3 latch fanin 13 timing value = 0.0 for cell sc1p3 at line 97
WhatDelayType: Warning! Unknown delay type sc1p3 at line 97 for ce
11 sc1p3

Warning! sc1p3 flipflop fanin 13 timing value = 0.0 for cell sc1p3 at line 97
WhatDelayType: Warning! Unknown delay type sc1p3 at line 97 for ce
11 sc1p3

Warning! sc1p3 latchlatch fanin 13 timing value = 0.0 for cell sc1p3 at line 97
WhatDelayType: Warning! Unknown delay type sc1p3 at line 97 for ce
11 sc1p3

Warning! sc1p3 hrflop fanin 13 timing value = 0.0 for cell sc1p3 at line 97
WhatDelayType: Warning! Unknown delay type sc1p3 at line 97 for ce
11 sc1p3

Warning! sc1p3 gate fanin 14 timing value = 0.0 for cell sc1p3 at line 97
WhatDelayType: Warning! Unknown delay type sc1p3 at line 97 for ce
11 sc1p3

Warning! sc1p3 latch fanin 14 timing value = 0.0 for cell sc1p3 at line 97
WhatDelayType: Warning! Unknown delay type sc1p3 at line 97 for ce
11 sc1p3

Warning! sc1p3 flipflop fanin 14 timing value = 0.0 for cell sc1p3 at line 97
WhatDelayType: Warning! Unknown delay type sc1p3 at line 97 for ce
11 sc1p3

Warning! sc1p3 latchlatch fanin 14 timing value = 0.0 for cell sc1p3 at line 97
WhatDelayType: Warning! Unknown delay type sc1p3 at line 97 for ce
11 sc1p3

Warning! sc1p3 hrflop fanin 14 timing value = 0.0 for cell sc1p3 at line 97
WhatDelayType: Warning! Unknown delay type sc1p3 at line 97 for ce
ll sc1p3

Warning! sc1p3 gate fanin 15 timing value = 0.0 for cell sc1p3 at line 97
WhatDelayType: Warning! Unknown delay type sc1p3 at line 97 for ce
ll sc1p3

Warning! sc1p3 latch fanin 15 timing value = 0.0 for cell sc1p3 at line 97
WhatDelayType: Warning! Unknown delay type sc1p3 at line 97 for ce
ll sc1p3

Warning! sc1p3 flipflop fanin 15 timing value = 0.0 for cell sc1p3 at line 97
WhatDelayType: Warning! Unknown delay type sc1p3 at line 97 for ce
ll sc1p3

Warning! sc1p3 latchlatch fanin 15 timing value = 0.0 for cell sc1p3 at line 97
WhatDelayType: Warning! Unknown delay type sc1p3 at line 97 for ce
ll sc1p3

Warning! sc1p3 hrflop fanin 15 timing value = 0.0 for cell sc1p3 at line 97
WhatDelayType: Warning! Unknown delay type sc1p3 at line 97 for ce
ll sc1p3

Warning! sc1p3 gate fanin 16 timing value = 0.0 for cell sc1p3 at line 97
WhatDelayType: Warning! Unknown delay type sc1p3 at line 97 for ce
ll sc1p3

Warning! sc1p3 latch fanin 16 timing value = 0.0 for cell sc1p3 at line 97
WhatDelayType: Warning! Unknown delay type sc1p3 at line 97 for ce
ll sc1p3

Warning! sc1p3 flipflop fanin 16 timing value = 0.0 for cell sc1p3 at line 97
WhatDelayType: Warning! Unknown delay type sc1p3 at line 97 for ce
ll sc1p3

Warning! sc1p3 latchlatch fanin 16 timing value = 0.0 for cell sc1p3 at line 97
WhatDelayType: Warning! Unknown delay type sc1p3 at line 97 for ce
ll sc1p3

Warning! sc1p3 hrflop fanin 16 timing value = 0.0 for cell sc1p3 at line 97
WhatDelayType: Warning! Unknown delay type sc1p3 at line 97 for ce
ll sc1p3

Warning! sc1p3 gate fanin 17 timing value = 0.0 for cell sc1p3 at line 97
WhatDelayType: Warning! Unknown delay type sc1p3 at line 97 for ce
ll sc1p3

Warning! sc1p3 latch fanin 17 timing value = 0.0 for cell sc1p3 at line 97
WhatDelayType: Warning! Unknown delay type sc1p3 at line 97 for ce
ll sc1p3

Warning! sc1p3 flipflop fanin 17 timing value = 0.0 for cell sc1p3 at line 97
WhatDelayType: Warning! Unknown delay type sc1p3 at line 97 for ce
ll sc1p3

Warning! sc1p3 latchlatch fanin 17 timing value = 0.0 for cell sc1p3 at line 97
WhatDelayType: Warning! Unknown delay type sc1p3 at line 97 for ce

l1 sc1p3

Warning! sc1p3 hrflop fanin 17 timing value = 0.0 for cell sc1p3 at line 97
WhatDelayType: Warning! Unknown delay type sc1p8 at line 102 for ce
l1 sc1p3

Warning! sc1p8 gate fanin 1 timing value = 0.0 for cell sc1p3 at line 102
WhatDelayType: Warning! Unknown delay type sc1p8 at line 102 for ce
l1 sc1p3

Warning! sc1p8 latch fanin 1 timing value = 0.0 for cell sc1p3 at line 102
WhatDelayType: Warning! Unknown delay type sc1p8 at line 102 for ce
l1 sc1p3

Warning! sc1p8 flipflop fanin 1 timing value = 0.0 for cell sc1p3 at line 102
WhatDelayType: Warning! Unknown delay type sc1p8 at line 102 for ce
l1 sc1p3

Warning! sc1p8 latchlatch fanin 1 timing value = 0.0 for cell sc1p3 at line 102
WhatDelayType: Warning! Unknown delay type sc1p8 at line 102 for ce
l1 sc1p3

Warning! sc1p8 hrflop fanin 1 timing value = 0.0 for cell sc1p3 at line 102
WhatDelayType: Warning! Unknown delay type sc1p8 at line 102 for ce
l1 sc1p3

Warning! sc1p8 gate fanin 2 timing value = 0.0 for cell sc1p3 at line 102
WhatDelayType: Warning! Unknown delay type sc1p8 at line 102 for ce
l1 sc1p3

Warning! sc1p8 latch fanin 2 timing value = 0.0 for cell sc1p3 at line 102
WhatDelayType: Warning! Unknown delay type sc1p8 at line 102 for ce
l1 sc1p3

Warning! sc1p8 flipflop fanin 2 timing value = 0.0 for cell sc1p3 at line 102
WhatDelayType: Warning! Unknown delay type sc1p8 at line 102 for ce
l1 sc1p3

Warning! sc1p8 latchlatch fanin 2 timing value = 0.0 for cell sc1p3 at line 102
WhatDelayType: Warning! Unknown delay type sc1p8 at line 102 for ce
l1 sc1p3

Warning! sc1p8 hrflop fanin 2 timing value = 0.0 for cell sc1p3 at line 102
WhatDelayType: Warning! Unknown delay type sc1p8 at line 102 for ce
l1 sc1p3

Warning! sc1p8 gate fanin 3 timing value = 0.0 for cell sc1p3 at line 102
WhatDelayType: Warning! Unknown delay type sc1p8 at line 102 for ce
l1 sc1p3

Warning! sc1p8 latch fanin 3 timing value = 0.0 for cell sc1p3 at line 102
WhatDelayType: Warning! Unknown delay type sc1p8 at line 102 for ce
l1 sc1p3

Warning! sc1p8 flipflop fanin 3 timing value = 0.0 for cell sc1p3 at line 102
WhatDelayType: Warning! Unknown delay type sc1p8 at line 102 for ce
l1 sc1p3

Warning! sc1p8 latchlatch fanin 3 timing value = 0.0 for cell sc1p3 at line 102

WhatDelayType: Warning! Unknown delay type sc1p8 at line 102 for ce
l1 sc1p3

Warning! sc1p8 hrflop fanin 3 timing value = 0.0 for cell sc1p3 at line
102

WhatDelayType: Warning! Unknown delay type sc1p8 at line 102 for ce
l1 sc1p3

Warning! sc1p8 gate fanin 4 timing value = 0.0 for cell sc1p3 at line 102

WhatDelayType: Warning! Unknown delay type sc1p8 at line 102 for ce
l1 sc1p3

Warning! sc1p8 latch fanin 4 timing value = 0.0 for cell sc1p3 at line 102

WhatDelayType: Warning! Unknown delay type sc1p8 at line 102 for ce
l1 sc1p3

Warning! sc1p8 flipflop fanin 4 timing value = 0.0 for cell sc1p3 at line
102

WhatDelayType: Warning! Unknown delay type sc1p8 at line 102 for ce
l1 sc1p3

Warning! sc1p8 latchlatch fanin 4 timing value = 0.0 for cell sc1p3 at
line 102

WhatDelayType: Warning! Unknown delay type sc1p8 at line 102 for ce
l1 sc1p3

Warning! sc1p8 hrflop fanin 4 timing value = 0.0 for cell sc1p3 at line
102

WhatDelayType: Warning! Unknown delay type sc1p8 at line 102 for ce
l1 sc1p3

Warning! sc1p8 gate fanin 5 timing value = 0.0 for cell sc1p3 at line 102

WhatDelayType: Warning! Unknown delay type sc1p8 at line 102 for ce
l1 sc1p3

Warning! sc1p8 latch fanin 5 timing value = 0.0 for cell sc1p3 at line 102

WhatDelayType: Warning! Unknown delay type sc1p8 at line 102 for ce
l1 sc1p3

Warning! sc1p8 flipflop fanin 5 timing value = 0.0 for cell sc1p3 at line
102

WhatDelayType: Warning! Unknown delay type sc1p8 at line 102 for ce
l1 sc1p3

Warning! sc1p8 latchlatch fanin 5 timing value = 0.0 for cell sc1p3 at
line 102

WhatDelayType: Warning! Unknown delay type sc1p8 at line 102 for ce
l1 sc1p3

Warning! sc1p8 hrflop fanin 5 timing value = 0.0 for cell sc1p3 at line
102

WhatDelayType: Warning! Unknown delay type sc1p8 at line 102 for ce
l1 sc1p3

Warning! sc1p8 gate fanin 6 timing value = 0.0 for cell sc1p3 at line 102

WhatDelayType: Warning! Unknown delay type sc1p8 at line 102 for ce
l1 sc1p3

Warning! sc1p8 latch fanin 6 timing value = 0.0 for cell sc1p3 at line 102

WhatDelayType: Warning! Unknown delay type sc1p8 at line 102 for ce
l1 sc1p3

Warning! sc1p8 flipflop fanin 6 timing value = 0.0 for cell sc1p3 at line
102

WhatDelayType: Warning! Unknown delay type sc1p8 at line 102 for ce
l1 sc1p3

Warning! sc1p8 latchlatch fanin 6 timing value = 0.0 for cell sc1p3 at

line 102
WhatDelayType: Warning! Unknown delay type sc1p8 at line 102 for ce
l1 sc1p3

Warning! sc1p8 hrflop fanin 6 timing value = 0.0 for cell sc1p3 at line
102
WhatDelayType: Warning! Unknown delay type sc1p8 at line 102 for ce
l1 sc1p3

Warning! sc1p8 gate fanin 7 timing value = 0.0 for cell sc1p3 at line 102
WhatDelayType: Warning! Unknown delay type sc1p8 at line 102 for ce
l1 sc1p3

Warning! sc1p8 latch fanin 7 timing value = 0.0 for cell sc1p3 at line 102
WhatDelayType: Warning! Unknown delay type sc1p8 at line 102 for ce
l1 sc1p3

Warning! sc1p8 flipflop fanin 7 timing value = 0.0 for cell sc1p3 at line
102
WhatDelayType: Warning! Unknown delay type sc1p8 at line 102 for ce
l1 sc1p3

Warning! sc1p8 latchlatch fanin 7 timing value = 0.0 for cell sc1p3 at
line 102
WhatDelayType: Warning! Unknown delay type sc1p8 at line 102 for ce
l1 sc1p3

Warning! sc1p8 hrflop fanin 7 timing value = 0.0 for cell sc1p3 at line
102
WhatDelayType: Warning! Unknown delay type sc1p8 at line 102 for ce
l1 sc1p3

Warning! sc1p8 gate fanin 8 timing value = 0.0 for cell sc1p3 at line 102
WhatDelayType: Warning! Unknown delay type sc1p8 at line 102 for ce
l1 sc1p3

Warning! sc1p8 latch fanin 8 timing value = 0.0 for cell sc1p3 at line 102
WhatDelayType: Warning! Unknown delay type sc1p8 at line 102 for ce
l1 sc1p3

Warning! sc1p8 flipflop fanin 8 timing value = 0.0 for cell sc1p3 at line
102
WhatDelayType: Warning! Unknown delay type sc1p8 at line 102 for ce
l1 sc1p3

Warning! sc1p8 latchlatch fanin 8 timing value = 0.0 for cell sc1p3 at
line 102
WhatDelayType: Warning! Unknown delay type sc1p8 at line 102 for ce
l1 sc1p3

Warning! sc1p8 hrflop fanin 8 timing value = 0.0 for cell sc1p3 at line
102
WhatDelayType: Warning! Unknown delay type sc1p8 at line 102 for ce
l1 sc1p3

Warning! sc1p8 gate fanin 9 timing value = 0.0 for cell sc1p3 at line 102
WhatDelayType: Warning! Unknown delay type sc1p8 at line 102 for ce
l1 sc1p3

Warning! sc1p8 latch fanin 9 timing value = 0.0 for cell sc1p3 at line 102
WhatDelayType: Warning! Unknown delay type sc1p8 at line 102 for ce
l1 sc1p3

Warning! sc1p8 flipflop fanin 9 timing value = 0.0 for cell sc1p3 at line
102
WhatDelayType: Warning! Unknown delay type sc1p8 at line 102 for ce
l1 sc1p3

Warning! sc1p8 latchlatch fanin 9 timing value = 0.0 for cell sc1p3 at line 102
WhatDelayType: Warning! Unknown delay type sc1p8 at line 102 for ce
l1 sc1p3

Warning! sc1p8 hrflop fanin 9 timing value = 0.0 for cell sc1p3 at line 102
WhatDelayType: Warning! Unknown delay type sc1p8 at line 102 for ce
l1 sc1p3

Warning! sc1p8 gate fanin 10 timing value = 0.0 for cell sc1p3 at line 102
WhatDelayType: Warning! Unknown delay type sc1p8 at line 102 for ce
l1 sc1p3

Warning! sc1p8 latch fanin 10 timing value = 0.0 for cell sc1p3 at line 102
WhatDelayType: Warning! Unknown delay type sc1p8 at line 102 for ce
l1 sc1p3

Warning! sc1p8 flipflop fanin 10 timing value = 0.0 for cell sc1p3 at line 102
WhatDelayType: Warning! Unknown delay type sc1p8 at line 102 for ce
l1 sc1p3

Warning! sc1p8 latchlatch fanin 10 timing value = 0.0 for cell sc1p3 at line 102
WhatDelayType: Warning! Unknown delay type sc1p8 at line 102 for ce
l1 sc1p3

Warning! sc1p8 hrflop fanin 10 timing value = 0.0 for cell sc1p3 at line 102
WhatDelayType: Warning! Unknown delay type sc1p8 at line 102 for ce
l1 sc1p3

Warning! sc1p8 gate fanin 11 timing value = 0.0 for cell sc1p3 at line 102
WhatDelayType: Warning! Unknown delay type sc1p8 at line 102 for ce
l1 sc1p3

Warning! sc1p8 latch fanin 11 timing value = 0.0 for cell sc1p3 at line 102
WhatDelayType: Warning! Unknown delay type sc1p8 at line 102 for ce
l1 sc1p3

Warning! sc1p8 flipflop fanin 11 timing value = 0.0 for cell sc1p3 at line 102
WhatDelayType: Warning! Unknown delay type sc1p8 at line 102 for ce
l1 sc1p3

Warning! sc1p8 latchlatch fanin 11 timing value = 0.0 for cell sc1p3 at line 102
WhatDelayType: Warning! Unknown delay type sc1p8 at line 102 for ce
l1 sc1p3

Warning! sc1p8 hrflop fanin 11 timing value = 0.0 for cell sc1p3 at line 102
WhatDelayType: Warning! Unknown delay type sc1p8 at line 102 for ce
l1 sc1p3

Warning! sc1p8 gate fanin 12 timing value = 0.0 for cell sc1p3 at line 102
WhatDelayType: Warning! Unknown delay type sc1p8 at line 102 for ce
l1 sc1p3

Warning! sc1p8 latch fanin 12 timing value = 0.0 for cell sc1p3 at line 102
WhatDelayType: Warning! Unknown delay type sc1p8 at line 102 for ce
l1 sc1p3

Warning! sc1p8 flipflop fanin 12 timing value = 0.0 for cell sc1p3 at line

102
WhatDelayType: Warning! Unknown delay type sc1p8 at line 102 for ce
l1 sc1p3

Warning! sc1p8 latchlatch fanin 12 timing value = 0.0 for cell sc1p3 at
line 102
WhatDelayType: Warning! Unknown delay type sc1p8 at line 102 for ce
l1 sc1p3

Warning! sc1p8 hrflop fanin 12 timing value = 0.0 for cell sc1p3 at line
102
WhatDelayType: Warning! Unknown delay type sc1p8 at line 102 for ce
l1 sc1p3

Warning! sc1p8 gate fanin 13 timing value = 0.0 for cell sc1p3 at line 102
WhatDelayType: Warning! Unknown delay type sc1p8 at line 102 for ce
l1 sc1p3

Warning! sc1p8 latch fanin 13 timing value = 0.0 for cell sc1p3 at line
102
WhatDelayType: Warning! Unknown delay type sc1p8 at line 102 for ce
l1 sc1p3

Warning! sc1p8 flipflop fanin 13 timing value = 0.0 for cell sc1p3 at line
102
WhatDelayType: Warning! Unknown delay type sc1p8 at line 102 for ce
l1 sc1p3

Warning! sc1p8 latchlatch fanin 13 timing value = 0.0 for cell sc1p3 at
line 102
WhatDelayType: Warning! Unknown delay type sc1p8 at line 102 for ce
l1 sc1p3

Warning! sc1p8 hrflop fanin 13 timing value = 0.0 for cell sc1p3 at line
102
WhatDelayType: Warning! Unknown delay type sc1p8 at line 102 for ce
l1 sc1p3

Warning! sc1p8 gate fanin 14 timing value = 0.0 for cell sc1p3 at line 102
WhatDelayType: Warning! Unknown delay type sc1p8 at line 102 for ce
l1 sc1p3

Warning! sc1p8 latch fanin 14 timing value = 0.0 for cell sc1p3 at line
102
WhatDelayType: Warning! Unknown delay type sc1p8 at line 102 for ce
l1 sc1p3

Warning! sc1p8 flipflop fanin 14 timing value = 0.0 for cell sc1p3 at line
102
WhatDelayType: Warning! Unknown delay type sc1p8 at line 102 for ce
l1 sc1p3

Warning! sc1p8 latchlatch fanin 14 timing value = 0.0 for cell sc1p3 at
line 102
WhatDelayType: Warning! Unknown delay type sc1p8 at line 102 for ce
l1 sc1p3

Warning! sc1p8 hrflop fanin 14 timing value = 0.0 for cell sc1p3 at line
102
WhatDelayType: Warning! Unknown delay type sc1p8 at line 102 for ce
l1 sc1p3

Warning! sc1p8 gate fanin 15 timing value = 0.0 for cell sc1p3 at line 102
WhatDelayType: Warning! Unknown delay type sc1p8 at line 102 for ce
l1 sc1p3

Warning! sc1p8 latch fanin 15 timing value = 0.0 for cell sc1p3 at line
102

WhatDelayType: Warning! Unknown delay type sc1p8 at line 102 for ce
ll sc1p3

Warning! sc1p8 flipflop fanin 15 timing value = 0.0 for cell sc1p3 at line
102

WhatDelayType: Warning! Unknown delay type sc1p8 at line 102 for ce
ll sc1p3

Warning! sc1p8 latchlatch fanin 15 timing value = 0.0 for cell sc1p3 at
line 102

WhatDelayType: Warning! Unknown delay type sc1p8 at line 102 for ce
ll sc1p3

Warning! sc1p8 hrflop fanin 15 timing value = 0.0 for cell sc1p3 at line
102

WhatDelayType: Warning! Unknown delay type sc1p8 at line 102 for ce
ll sc1p3

Warning! sc1p8 gate fanin 16 timing value = 0.0 for cell sc1p3 at line 102

WhatDelayType: Warning! Unknown delay type sc1p8 at line 102 for ce
ll sc1p3

Warning! sc1p8 latch fanin 16 timing value = 0.0 for cell sc1p3 at line
102

WhatDelayType: Warning! Unknown delay type sc1p8 at line 102 for ce
ll sc1p3

Warning! sc1p8 flipflop fanin 16 timing value = 0.0 for cell sc1p3 at line
102

WhatDelayType: Warning! Unknown delay type sc1p8 at line 102 for ce
ll sc1p3

Warning! sc1p8 latchlatch fanin 16 timing value = 0.0 for cell sc1p3 at
line 102

WhatDelayType: Warning! Unknown delay type sc1p8 at line 102 for ce
ll sc1p3

Warning! sc1p8 hrflop fanin 16 timing value = 0.0 for cell sc1p3 at line
102

WhatDelayType: Warning! Unknown delay type sc1p8 at line 102 for ce
ll sc1p3

Warning! sc1p8 gate fanin 17 timing value = 0.0 for cell sc1p3 at line 102

WhatDelayType: Warning! Unknown delay type sc1p8 at line 102 for ce
ll sc1p3

Warning! sc1p8 latch fanin 17 timing value = 0.0 for cell sc1p3 at line
102

WhatDelayType: Warning! Unknown delay type sc1p8 at line 102 for ce
ll sc1p3

Warning! sc1p8 flipflop fanin 17 timing value = 0.0 for cell sc1p3 at line
102

WhatDelayType: Warning! Unknown delay type sc1p8 at line 102 for ce
ll sc1p3

Warning! sc1p8 latchlatch fanin 17 timing value = 0.0 for cell sc1p3 at
line 102

WhatDelayType: Warning! Unknown delay type sc1p8 at line 102 for ce
ll sc1p3

Warning! sc1p8 hrflop fanin 17 timing value = 0.0 for cell sc1p3 at line
102

WhatDelayType: Warning! Unknown delay type sc2p3 at line 107 for ce
ll sc1p3

Warning! sc2p3 gate fanin 1 timing value = 0.0 for cell sc1p3 at line 107

WhatDelayType: Warning! Unknown delay type sc2p3 at line 107 for ce

ll sc1p3

Warning! sc2p3 latch fanin 1 timing value = 0.0 for cell sc1p3 at line 107
WhatDelayType: Warning! Unknown delay type sc2p3 at line 107 for ce
ll sc1p3

Warning! sc2p3 flipflop fanin 1 timing value = 0.0 for cell sc1p3 at line 107
WhatDelayType: Warning! Unknown delay type sc2p3 at line 107 for ce
ll sc1p3

Warning! sc2p3 latchlatch fanin 1 timing value = 0.0 for cell sc1p3 at line 107
WhatDelayType: Warning! Unknown delay type sc2p3 at line 107 for ce
ll sc1p3

Warning! sc2p3 hrflop fanin 1 timing value = 0.0 for cell sc1p3 at line 107
WhatDelayType: Warning! Unknown delay type sc2p3 at line 107 for ce
ll sc1p3

Warning! sc2p3 gate fanin 2 timing value = 0.0 for cell sc1p3 at line 107
WhatDelayType: Warning! Unknown delay type sc2p3 at line 107 for ce
ll sc1p3

Warning! sc2p3 latch fanin 2 timing value = 0.0 for cell sc1p3 at line 107
WhatDelayType: Warning! Unknown delay type sc2p3 at line 107 for ce
ll sc1p3

Warning! sc2p3 flipflop fanin 2 timing value = 0.0 for cell sc1p3 at line 107
WhatDelayType: Warning! Unknown delay type sc2p3 at line 107 for ce
ll sc1p3

Warning! sc2p3 latchlatch fanin 2 timing value = 0.0 for cell sc1p3 at line 107
WhatDelayType: Warning! Unknown delay type sc2p3 at line 107 for ce
ll sc1p3

Warning! sc2p3 hrflop fanin 2 timing value = 0.0 for cell sc1p3 at line 107
WhatDelayType: Warning! Unknown delay type sc2p3 at line 107 for ce
ll sc1p3

Warning! sc2p3 gate fanin 3 timing value = 0.0 for cell sc1p3 at line 107
WhatDelayType: Warning! Unknown delay type sc2p3 at line 107 for ce
ll sc1p3

Warning! sc2p3 latch fanin 3 timing value = 0.0 for cell sc1p3 at line 107
WhatDelayType: Warning! Unknown delay type sc2p3 at line 107 for ce
ll sc1p3

Warning! sc2p3 flipflop fanin 3 timing value = 0.0 for cell sc1p3 at line 107
WhatDelayType: Warning! Unknown delay type sc2p3 at line 107 for ce
ll sc1p3

Warning! sc2p3 latchlatch fanin 3 timing value = 0.0 for cell sc1p3 at line 107
WhatDelayType: Warning! Unknown delay type sc2p3 at line 107 for ce
ll sc1p3

Warning! sc2p3 hrflop fanin 3 timing value = 0.0 for cell sc1p3 at line 107
WhatDelayType: Warning! Unknown delay type sc2p3 at line 107 for ce
ll sc1p3

Warning! sc2p3 gate fanin 4 timing value = 0.0 for cell sc1p3 at line 107

WhatDelayType: Warning! Unknown delay type sc2p3 at line 107 for ce
l1 sc1p3

Warning! sc2p3 latch fanin 4 timing value = 0.0 for cell sc1p3 at line 107
WhatDelayType: Warning! Unknown delay type sc2p3 at line 107 for ce
l1 sc1p3

Warning! sc2p3 flipflop fanin 4 timing value = 0.0 for cell sc1p3 at line
107
WhatDelayType: Warning! Unknown delay type sc2p3 at line 107 for ce
l1 sc1p3

Warning! sc2p3 latchlatch fanin 4 timing value = 0.0 for cell sc1p3 at
line 107
WhatDelayType: Warning! Unknown delay type sc2p3 at line 107 for ce
l1 sc1p3

Warning! sc2p3 hrflop fanin 4 timing value = 0.0 for cell sc1p3 at line
107
WhatDelayType: Warning! Unknown delay type sc2p3 at line 107 for ce
l1 sc1p3

Warning! sc2p3 gate fanin 5 timing value = 0.0 for cell sc1p3 at line 107
WhatDelayType: Warning! Unknown delay type sc2p3 at line 107 for ce
l1 sc1p3

Warning! sc2p3 latch fanin 5 timing value = 0.0 for cell sc1p3 at line 107
WhatDelayType: Warning! Unknown delay type sc2p3 at line 107 for ce
l1 sc1p3

Warning! sc2p3 flipflop fanin 5 timing value = 0.0 for cell sc1p3 at line
107
WhatDelayType: Warning! Unknown delay type sc2p3 at line 107 for ce
l1 sc1p3

Warning! sc2p3 latchlatch fanin 5 timing value = 0.0 for cell sc1p3 at
line 107
WhatDelayType: Warning! Unknown delay type sc2p3 at line 107 for ce
l1 sc1p3

Warning! sc2p3 hrflop fanin 5 timing value = 0.0 for cell sc1p3 at line
107
WhatDelayType: Warning! Unknown delay type sc2p3 at line 107 for ce
l1 sc1p3

Warning! sc2p3 gate fanin 6 timing value = 0.0 for cell sc1p3 at line 107
WhatDelayType: Warning! Unknown delay type sc2p3 at line 107 for ce
l1 sc1p3

Warning! sc2p3 latch fanin 6 timing value = 0.0 for cell sc1p3 at line 107
WhatDelayType: Warning! Unknown delay type sc2p3 at line 107 for ce
l1 sc1p3

Warning! sc2p3 flipflop fanin 6 timing value = 0.0 for cell sc1p3 at line
107
WhatDelayType: Warning! Unknown delay type sc2p3 at line 107 for ce
l1 sc1p3

Warning! sc2p3 latchlatch fanin 6 timing value = 0.0 for cell sc1p3 at
line 107
WhatDelayType: Warning! Unknown delay type sc2p3 at line 107 for ce
l1 sc1p3

Warning! sc2p3 hrflop fanin 6 timing value = 0.0 for cell sc1p3 at line
107
WhatDelayType: Warning! Unknown delay type sc2p3 at line 107 for ce
l1 sc1p3

Warning! sc2p3 gate fanin 7 timing value = 0.0 for cell sc1p3 at line 107
WhatDelayType: Warning! Unknown delay type sc2p3 at line 107 for ce
l1 sc1p3

Warning! sc2p3 latch fanin 7 timing value = 0.0 for cell sc1p3 at line 107
WhatDelayType: Warning! Unknown delay type sc2p3 at line 107 for ce
l1 sc1p3

Warning! sc2p3 flipflop fanin 7 timing value = 0.0 for cell sc1p3 at line 107
WhatDelayType: Warning! Unknown delay type sc2p3 at line 107 for ce
l1 sc1p3

Warning! sc2p3 latchlatch fanin 7 timing value = 0.0 for cell sc1p3 at line 107
WhatDelayType: Warning! Unknown delay type sc2p3 at line 107 for ce
l1 sc1p3

Warning! sc2p3 hrflop fanin 7 timing value = 0.0 for cell sc1p3 at line 107
WhatDelayType: Warning! Unknown delay type sc2p3 at line 107 for ce
l1 sc1p3

Warning! sc2p3 gate fanin 8 timing value = 0.0 for cell sc1p3 at line 107
WhatDelayType: Warning! Unknown delay type sc2p3 at line 107 for ce
l1 sc1p3

Warning! sc2p3 latch fanin 8 timing value = 0.0 for cell sc1p3 at line 107
WhatDelayType: Warning! Unknown delay type sc2p3 at line 107 for ce
l1 sc1p3

Warning! sc2p3 flipflop fanin 8 timing value = 0.0 for cell sc1p3 at line 107
WhatDelayType: Warning! Unknown delay type sc2p3 at line 107 for ce
l1 sc1p3

Warning! sc2p3 latchlatch fanin 8 timing value = 0.0 for cell sc1p3 at line 107
WhatDelayType: Warning! Unknown delay type sc2p3 at line 107 for ce
l1 sc1p3

Warning! sc2p3 hrflop fanin 8 timing value = 0.0 for cell sc1p3 at line 107
WhatDelayType: Warning! Unknown delay type sc2p3 at line 107 for ce
l1 sc1p3

Warning! sc2p3 gate fanin 9 timing value = 0.0 for cell sc1p3 at line 107
WhatDelayType: Warning! Unknown delay type sc2p3 at line 107 for ce
l1 sc1p3

Warning! sc2p3 latch fanin 9 timing value = 0.0 for cell sc1p3 at line 107
WhatDelayType: Warning! Unknown delay type sc2p3 at line 107 for ce
l1 sc1p3

Warning! sc2p3 flipflop fanin 9 timing value = 0.0 for cell sc1p3 at line 107
WhatDelayType: Warning! Unknown delay type sc2p3 at line 107 for ce
l1 sc1p3

Warning! sc2p3 latchlatch fanin 9 timing value = 0.0 for cell sc1p3 at line 107
WhatDelayType: Warning! Unknown delay type sc2p3 at line 107 for ce
l1 sc1p3

Warning! sc2p3 hrflop fanin 9 timing value = 0.0 for cell sc1p3 at line 107
WhatDelayType: Warning! Unknown delay type sc2p3 at line 107 for ce
l1 sc1p3

Warning! sc2p3 gate fanin 10 timing value = 0.0 for cell sc1p3 at line 107
WhatDelayType: Warning! Unknown delay type sc2p3 at line 107 for ce
ll sc1p3

Warning! sc2p3 latch fanin 10 timing value = 0.0 for cell sc1p3 at line 107
WhatDelayType: Warning! Unknown delay type sc2p3 at line 107 for ce
ll sc1p3

Warning! sc2p3 flipflop fanin 10 timing value = 0.0 for cell sc1p3 at line 107
WhatDelayType: Warning! Unknown delay type sc2p3 at line 107 for ce
ll sc1p3

Warning! sc2p3 latchlatch fanin 10 timing value = 0.0 for cell sc1p3 at line 107
WhatDelayType: Warning! Unknown delay type sc2p3 at line 107 for ce
ll sc1p3

Warning! sc2p3 hrflop fanin 10 timing value = 0.0 for cell sc1p3 at line 107
WhatDelayType: Warning! Unknown delay type sc2p3 at line 107 for ce
ll sc1p3

Warning! sc2p3 gate fanin 11 timing value = 0.0 for cell sc1p3 at line 107
WhatDelayType: Warning! Unknown delay type sc2p3 at line 107 for ce
ll sc1p3

Warning! sc2p3 latch fanin 11 timing value = 0.0 for cell sc1p3 at line 107
WhatDelayType: Warning! Unknown delay type sc2p3 at line 107 for ce
ll sc1p3

Warning! sc2p3 flipflop fanin 11 timing value = 0.0 for cell sc1p3 at line 107
WhatDelayType: Warning! Unknown delay type sc2p3 at line 107 for ce
ll sc1p3

Warning! sc2p3 latchlatch fanin 11 timing value = 0.0 for cell sc1p3 at line 107
WhatDelayType: Warning! Unknown delay type sc2p3 at line 107 for ce
ll sc1p3

Warning! sc2p3 hrflop fanin 11 timing value = 0.0 for cell sc1p3 at line 107
WhatDelayType: Warning! Unknown delay type sc2p3 at line 107 for ce
ll sc1p3

Warning! sc2p3 gate fanin 12 timing value = 0.0 for cell sc1p3 at line 107
WhatDelayType: Warning! Unknown delay type sc2p3 at line 107 for ce
ll sc1p3

Warning! sc2p3 latch fanin 12 timing value = 0.0 for cell sc1p3 at line 107
WhatDelayType: Warning! Unknown delay type sc2p3 at line 107 for ce
ll sc1p3

Warning! sc2p3 flipflop fanin 12 timing value = 0.0 for cell sc1p3 at line 107
WhatDelayType: Warning! Unknown delay type sc2p3 at line 107 for ce
ll sc1p3

Warning! sc2p3 latchlatch fanin 12 timing value = 0.0 for cell sc1p3 at line 107
WhatDelayType: Warning! Unknown delay type sc2p3 at line 107 for ce
ll sc1p3

Warning! sc2p3 hrflop fanin 12 timing value = 0.0 for cell sc1p3 at line 107
WhatDelayType: Warning! Unknown delay type sc2p3 at line 107 for ce
l1 sc1p3

Warning! sc2p3 gate fanin 13 timing value = 0.0 for cell sc1p3 at line 107
WhatDelayType: Warning! Unknown delay type sc2p3 at line 107 for ce
l1 sc1p3

Warning! sc2p3 latch fanin 13 timing value = 0.0 for cell sc1p3 at line 107
WhatDelayType: Warning! Unknown delay type sc2p3 at line 107 for ce
l1 sc1p3

Warning! sc2p3 flipflop fanin 13 timing value = 0.0 for cell sc1p3 at line 107
WhatDelayType: Warning! Unknown delay type sc2p3 at line 107 for ce
l1 sc1p3

Warning! sc2p3 latchlatch fanin 13 timing value = 0.0 for cell sc1p3 at line 107
WhatDelayType: Warning! Unknown delay type sc2p3 at line 107 for ce
l1 sc1p3

Warning! sc2p3 hrflop fanin 13 timing value = 0.0 for cell sc1p3 at line 107
WhatDelayType: Warning! Unknown delay type sc2p3 at line 107 for ce
l1 sc1p3

Warning! sc2p3 gate fanin 14 timing value = 0.0 for cell sc1p3 at line 107
WhatDelayType: Warning! Unknown delay type sc2p3 at line 107 for ce
l1 sc1p3

Warning! sc2p3 latch fanin 14 timing value = 0.0 for cell sc1p3 at line 107
WhatDelayType: Warning! Unknown delay type sc2p3 at line 107 for ce
l1 sc1p3

Warning! sc2p3 flipflop fanin 14 timing value = 0.0 for cell sc1p3 at line 107
WhatDelayType: Warning! Unknown delay type sc2p3 at line 107 for ce
l1 sc1p3

Warning! sc2p3 latchlatch fanin 14 timing value = 0.0 for cell sc1p3 at line 107
WhatDelayType: Warning! Unknown delay type sc2p3 at line 107 for ce
l1 sc1p3

Warning! sc2p3 hrflop fanin 14 timing value = 0.0 for cell sc1p3 at line 107
WhatDelayType: Warning! Unknown delay type sc2p3 at line 107 for ce
l1 sc1p3

Warning! sc2p3 gate fanin 15 timing value = 0.0 for cell sc1p3 at line 107
WhatDelayType: Warning! Unknown delay type sc2p3 at line 107 for ce
l1 sc1p3

Warning! sc2p3 latch fanin 15 timing value = 0.0 for cell sc1p3 at line 107
WhatDelayType: Warning! Unknown delay type sc2p3 at line 107 for ce
l1 sc1p3

Warning! sc2p3 flipflop fanin 15 timing value = 0.0 for cell sc1p3 at line 107
WhatDelayType: Warning! Unknown delay type sc2p3 at line 107 for ce
l1 sc1p3

Warning! sc2p3 latchlatch fanin 15 timing value = 0.0 for cell sc1p3 at

line 107
WhatDelayType: Warning! Unknown delay type sc2p3 at line 107 for ce
l1 sclp3

Warning! sc2p3 hrflop fanin 15 timing value = 0.0 for cell sclp3 at line
107
WhatDelayType: Warning! Unknown delay type sc2p3 at line 107 for ce
l1 sclp3

Warning! sc2p3 gate fanin 16 timing value = 0.0 for cell sclp3 at line 107
WhatDelayType: Warning! Unknown delay type sc2p3 at line 107 for ce
l1 sclp3

Warning! sc2p3 latch fanin 16 timing value = 0.0 for cell sclp3 at line
107
WhatDelayType: Warning! Unknown delay type sc2p3 at line 107 for ce
l1 sclp3

Warning! sc2p3 flipflop fanin 16 timing value = 0.0 for cell sclp3 at line
107
WhatDelayType: Warning! Unknown delay type sc2p3 at line 107 for ce
l1 sclp3

Warning! sc2p3 latchlatch fanin 16 timing value = 0.0 for cell sclp3 at
line 107
WhatDelayType: Warning! Unknown delay type sc2p3 at line 107 for ce
l1 sclp3

Warning! sc2p3 hrflop fanin 16 timing value = 0.0 for cell sclp3 at line
107
WhatDelayType: Warning! Unknown delay type sc2p3 at line 107 for ce
l1 sclp3

Warning! sc2p3 gate fanin 17 timing value = 0.0 for cell sclp3 at line 107
WhatDelayType: Warning! Unknown delay type sc2p3 at line 107 for ce
l1 sclp3

Warning! sc2p3 latch fanin 17 timing value = 0.0 for cell sclp3 at line
107
WhatDelayType: Warning! Unknown delay type sc2p3 at line 107 for ce
l1 sclp3

Warning! sc2p3 flipflop fanin 17 timing value = 0.0 for cell sclp3 at line
107
WhatDelayType: Warning! Unknown delay type sc2p3 at line 107 for ce
l1 sclp3

Warning! sc2p3 latchlatch fanin 17 timing value = 0.0 for cell sclp3 at
line 107
WhatDelayType: Warning! Unknown delay type sc2p3 at line 107 for ce
l1 sclp3

Warning! sc2p3 hrflop fanin 17 timing value = 0.0 for cell sclp3 at line
107
WhatDelayType: Warning! Unknown delay type sc2p8 at line 112 for ce
l1 sclp3

Warning! sc2p8 gate fanin 1 timing value = 0.0 for cell sclp3 at line 112
WhatDelayType: Warning! Unknown delay type sc2p8 at line 112 for ce
l1 sclp3

Warning! sc2p8 latch fanin 1 timing value = 0.0 for cell sclp3 at line 112
WhatDelayType: Warning! Unknown delay type sc2p8 at line 112 for ce
l1 sclp3

Warning! sc2p8 flipflop fanin 1 timing value = 0.0 for cell sclp3 at line
112
WhatDelayType: Warning! Unknown delay type sc2p8 at line 112 for ce

l1 sc1p3

Warning! sc2p8 latchlatch fanin 1 timing value = 0.0 for cell sc1p3 at line 112

WhatDelayType: Warning! Unknown delay type sc2p8 at line 112 for ce
l1 sc1p3

Warning! sc2p8 hrflop fanin 1 timing value = 0.0 for cell sc1p3 at line 112

WhatDelayType: Warning! Unknown delay type sc2p8 at line 112 for ce
l1 sc1p3

Warning! sc2p8 gate fanin 2 timing value = 0.0 for cell sc1p3 at line 112

WhatDelayType: Warning! Unknown delay type sc2p8 at line 112 for ce
l1 sc1p3

Warning! sc2p8 latch fanin 2 timing value = 0.0 for cell sc1p3 at line 112

WhatDelayType: Warning! Unknown delay type sc2p8 at line 112 for ce
l1 sc1p3

Warning! sc2p8 flipflop fanin 2 timing value = 0.0 for cell sc1p3 at line 112

WhatDelayType: Warning! Unknown delay type sc2p8 at line 112 for ce
l1 sc1p3

Warning! sc2p8 latchlatch fanin 2 timing value = 0.0 for cell sc1p3 at line 112

WhatDelayType: Warning! Unknown delay type sc2p8 at line 112 for ce
l1 sc1p3

Warning! sc2p8 hrflop fanin 2 timing value = 0.0 for cell sc1p3 at line 112

WhatDelayType: Warning! Unknown delay type sc2p8 at line 112 for ce
l1 sc1p3

Warning! sc2p8 gate fanin 3 timing value = 0.0 for cell sc1p3 at line 112

WhatDelayType: Warning! Unknown delay type sc2p8 at line 112 for ce
l1 sc1p3

Warning! sc2p8 latch fanin 3 timing value = 0.0 for cell sc1p3 at line 112

WhatDelayType: Warning! Unknown delay type sc2p8 at line 112 for ce
l1 sc1p3

Warning! sc2p8 flipflop fanin 3 timing value = 0.0 for cell sc1p3 at line 112

WhatDelayType: Warning! Unknown delay type sc2p8 at line 112 for ce
l1 sc1p3

Warning! sc2p8 latchlatch fanin 3 timing value = 0.0 for cell sc1p3 at line 112

WhatDelayType: Warning! Unknown delay type sc2p8 at line 112 for ce
l1 sc1p3

Warning! sc2p8 hrflop fanin 3 timing value = 0.0 for cell sc1p3 at line 112

WhatDelayType: Warning! Unknown delay type sc2p8 at line 112 for ce
l1 sc1p3

Warning! sc2p8 gate fanin 4 timing value = 0.0 for cell sc1p3 at line 112

WhatDelayType: Warning! Unknown delay type sc2p8 at line 112 for ce
l1 sc1p3

Warning! sc2p8 latch fanin 4 timing value = 0.0 for cell sc1p3 at line 112

WhatDelayType: Warning! Unknown delay type sc2p8 at line 112 for ce
l1 sc1p3

Warning! sc2p8 flipflop fanin 4 timing value = 0.0 for cell sc1p3 at line 112

WhatDelayType: Warning! Unknown delay type sc2p8 at line 112 for ce
l1 sc1p3

Warning! sc2p8 latchlatch fanin 4 timing value = 0.0 for cell sc1p3 at
line 112

WhatDelayType: Warning! Unknown delay type sc2p8 at line 112 for ce
l1 sc1p3

Warning! sc2p8 hrflop fanin 4 timing value = 0.0 for cell sc1p3 at line
112

WhatDelayType: Warning! Unknown delay type sc2p8 at line 112 for ce
l1 sc1p3

Warning! sc2p8 gate fanin 5 timing value = 0.0 for cell sc1p3 at line 112

WhatDelayType: Warning! Unknown delay type sc2p8 at line 112 for ce
l1 sc1p3

Warning! sc2p8 latch fanin 5 timing value = 0.0 for cell sc1p3 at line 112

WhatDelayType: Warning! Unknown delay type sc2p8 at line 112 for ce
l1 sc1p3

Warning! sc2p8 flipflop fanin 5 timing value = 0.0 for cell sc1p3 at line
112

WhatDelayType: Warning! Unknown delay type sc2p8 at line 112 for ce
l1 sc1p3

Warning! sc2p8 latchlatch fanin 5 timing value = 0.0 for cell sc1p3 at
line 112

WhatDelayType: Warning! Unknown delay type sc2p8 at line 112 for ce
l1 sc1p3

Warning! sc2p8 hrflop fanin 5 timing value = 0.0 for cell sc1p3 at line
112

WhatDelayType: Warning! Unknown delay type sc2p8 at line 112 for ce
l1 sc1p3

Warning! sc2p8 gate fanin 6 timing value = 0.0 for cell sc1p3 at line 112

WhatDelayType: Warning! Unknown delay type sc2p8 at line 112 for ce
l1 sc1p3

Warning! sc2p8 latch fanin 6 timing value = 0.0 for cell sc1p3 at line 112

WhatDelayType: Warning! Unknown delay type sc2p8 at line 112 for ce
l1 sc1p3

Warning! sc2p8 flipflop fanin 6 timing value = 0.0 for cell sc1p3 at line
112

WhatDelayType: Warning! Unknown delay type sc2p8 at line 112 for ce
l1 sc1p3

Warning! sc2p8 latchlatch fanin 6 timing value = 0.0 for cell sc1p3 at
line 112

WhatDelayType: Warning! Unknown delay type sc2p8 at line 112 for ce
l1 sc1p3

Warning! sc2p8 hrflop fanin 6 timing value = 0.0 for cell sc1p3 at line
112

WhatDelayType: Warning! Unknown delay type sc2p8 at line 112 for ce
l1 sc1p3

Warning! sc2p8 gate fanin 7 timing value = 0.0 for cell sc1p3 at line 112

WhatDelayType: Warning! Unknown delay type sc2p8 at line 112 for ce
l1 sc1p3

Warning! sc2p8 latch fanin 7 timing value = 0.0 for cell sc1p3 at line 112

WhatDelayType: Warning! Unknown delay type sc2p8 at line 112 for ce
l1 sc1p3

Warning! sc2p8 flipflop fanin 7 timing value = 0.0 for cell sc1p3 at line

112
WhatDelayType: Warning! Unknown delay type sc2p8 at line 112 for ce
l1 sc1p3

Warning! sc2p8 latchlatch fanin 7 timing value = 0.0 for cell sc1p3 at
line 112
WhatDelayType: Warning! Unknown delay type sc2p8 at line 112 for ce
l1 sc1p3

Warning! sc2p8 hrflop fanin 7 timing value = 0.0 for cell sc1p3 at line
112
WhatDelayType: Warning! Unknown delay type sc2p8 at line 112 for ce
l1 sc1p3

Warning! sc2p8 gate fanin 8 timing value = 0.0 for cell sc1p3 at line 112
WhatDelayType: Warning! Unknown delay type sc2p8 at line 112 for ce
l1 sc1p3

Warning! sc2p8 latch fanin 8 timing value = 0.0 for cell sc1p3 at line 112
WhatDelayType: Warning! Unknown delay type sc2p8 at line 112 for ce
l1 sc1p3

Warning! sc2p8 flipflop fanin 8 timing value = 0.0 for cell sc1p3 at line
112
WhatDelayType: Warning! Unknown delay type sc2p8 at line 112 for ce
l1 sc1p3

Warning! sc2p8 latchlatch fanin 8 timing value = 0.0 for cell sc1p3 at
line 112
WhatDelayType: Warning! Unknown delay type sc2p8 at line 112 for ce
l1 sc1p3

Warning! sc2p8 hrflop fanin 8 timing value = 0.0 for cell sc1p3 at line
112
WhatDelayType: Warning! Unknown delay type sc2p8 at line 112 for ce
l1 sc1p3

Warning! sc2p8 gate fanin 9 timing value = 0.0 for cell sc1p3 at line 112
WhatDelayType: Warning! Unknown delay type sc2p8 at line 112 for ce
l1 sc1p3

Warning! sc2p8 latch fanin 9 timing value = 0.0 for cell sc1p3 at line 112
WhatDelayType: Warning! Unknown delay type sc2p8 at line 112 for ce
l1 sc1p3

Warning! sc2p8 flipflop fanin 9 timing value = 0.0 for cell sc1p3 at line
112
WhatDelayType: Warning! Unknown delay type sc2p8 at line 112 for ce
l1 sc1p3

Warning! sc2p8 latchlatch fanin 9 timing value = 0.0 for cell sc1p3 at
line 112
WhatDelayType: Warning! Unknown delay type sc2p8 at line 112 for ce
l1 sc1p3

Warning! sc2p8 hrflop fanin 9 timing value = 0.0 for cell sc1p3 at line
112
WhatDelayType: Warning! Unknown delay type sc2p8 at line 112 for ce
l1 sc1p3

Warning! sc2p8 gate fanin 10 timing value = 0.0 for cell sc1p3 at line 112
WhatDelayType: Warning! Unknown delay type sc2p8 at line 112 for ce
l1 sc1p3

Warning! sc2p8 latch fanin 10 timing value = 0.0 for cell sc1p3 at line
112
WhatDelayType: Warning! Unknown delay type sc2p8 at line 112 for ce
l1 sc1p3

Warning! sc2p8 flipflop fanin 10 timing value = 0.0 for cell sc1p3 at line 112
WhatDelayType: Warning! Unknown delay type sc2p8 at line 112 for ce
l1 sc1p3

Warning! sc2p8 latchlatch fanin 10 timing value = 0.0 for cell sc1p3 at line 112
WhatDelayType: Warning! Unknown delay type sc2p8 at line 112 for ce
l1 sc1p3

Warning! sc2p8 hrflop fanin 10 timing value = 0.0 for cell sc1p3 at line 112
WhatDelayType: Warning! Unknown delay type sc2p8 at line 112 for ce
l1 sc1p3

Warning! sc2p8 gate fanin 11 timing value = 0.0 for cell sc1p3 at line 112
WhatDelayType: Warning! Unknown delay type sc2p8 at line 112 for ce
l1 sc1p3

Warning! sc2p8 latch fanin 11 timing value = 0.0 for cell sc1p3 at line 112
WhatDelayType: Warning! Unknown delay type sc2p8 at line 112 for ce
l1 sc1p3

Warning! sc2p8 flipflop fanin 11 timing value = 0.0 for cell sc1p3 at line 112
WhatDelayType: Warning! Unknown delay type sc2p8 at line 112 for ce
l1 sc1p3

Warning! sc2p8 latchlatch fanin 11 timing value = 0.0 for cell sc1p3 at line 112
WhatDelayType: Warning! Unknown delay type sc2p8 at line 112 for ce
l1 sc1p3

Warning! sc2p8 hrflop fanin 11 timing value = 0.0 for cell sc1p3 at line 112
WhatDelayType: Warning! Unknown delay type sc2p8 at line 112 for ce
l1 sc1p3

Warning! sc2p8 gate fanin 12 timing value = 0.0 for cell sc1p3 at line 112
WhatDelayType: Warning! Unknown delay type sc2p8 at line 112 for ce
l1 sc1p3

Warning! sc2p8 latch fanin 12 timing value = 0.0 for cell sc1p3 at line 112
WhatDelayType: Warning! Unknown delay type sc2p8 at line 112 for ce
l1 sc1p3

Warning! sc2p8 flipflop fanin 12 timing value = 0.0 for cell sc1p3 at line 112
WhatDelayType: Warning! Unknown delay type sc2p8 at line 112 for ce
l1 sc1p3

Warning! sc2p8 latchlatch fanin 12 timing value = 0.0 for cell sc1p3 at line 112
WhatDelayType: Warning! Unknown delay type sc2p8 at line 112 for ce
l1 sc1p3

Warning! sc2p8 hrflop fanin 12 timing value = 0.0 for cell sc1p3 at line 112
WhatDelayType: Warning! Unknown delay type sc2p8 at line 112 for ce
l1 sc1p3

Warning! sc2p8 gate fanin 13 timing value = 0.0 for cell sc1p3 at line 112
WhatDelayType: Warning! Unknown delay type sc2p8 at line 112 for ce
l1 sc1p3

Warning! sc2p8 latch fanin 13 timing value = 0.0 for cell sc1p3 at line
112
WhatDelayType: Warning! Unknown delay type sc2p8 at line 112 for ce
l1 sc1p3

Warning! sc2p8 flipflop fanin 13 timing value = 0.0 for cell sc1p3 at line
112
WhatDelayType: Warning! Unknown delay type sc2p8 at line 112 for ce
l1 sc1p3

Warning! sc2p8 latchlatch fanin 13 timing value = 0.0 for cell sc1p3 at
line 112
WhatDelayType: Warning! Unknown delay type sc2p8 at line 112 for ce
l1 sc1p3

Warning! sc2p8 hrflop fanin 13 timing value = 0.0 for cell sc1p3 at line
112
WhatDelayType: Warning! Unknown delay type sc2p8 at line 112 for ce
l1 sc1p3

Warning! sc2p8 gate fanin 14 timing value = 0.0 for cell sc1p3 at line 112
WhatDelayType: Warning! Unknown delay type sc2p8 at line 112 for ce
l1 sc1p3

Warning! sc2p8 latch fanin 14 timing value = 0.0 for cell sc1p3 at line
112
WhatDelayType: Warning! Unknown delay type sc2p8 at line 112 for ce
l1 sc1p3

Warning! sc2p8 flipflop fanin 14 timing value = 0.0 for cell sc1p3 at line
112
WhatDelayType: Warning! Unknown delay type sc2p8 at line 112 for ce
l1 sc1p3

Warning! sc2p8 latchlatch fanin 14 timing value = 0.0 for cell sc1p3 at
line 112
WhatDelayType: Warning! Unknown delay type sc2p8 at line 112 for ce
l1 sc1p3

Warning! sc2p8 hrflop fanin 14 timing value = 0.0 for cell sc1p3 at line
112
WhatDelayType: Warning! Unknown delay type sc2p8 at line 112 for ce
l1 sc1p3

Warning! sc2p8 gate fanin 15 timing value = 0.0 for cell sc1p3 at line 112
WhatDelayType: Warning! Unknown delay type sc2p8 at line 112 for ce
l1 sc1p3

Warning! sc2p8 latch fanin 15 timing value = 0.0 for cell sc1p3 at line
112
WhatDelayType: Warning! Unknown delay type sc2p8 at line 112 for ce
l1 sc1p3

Warning! sc2p8 flipflop fanin 15 timing value = 0.0 for cell sc1p3 at line
112
WhatDelayType: Warning! Unknown delay type sc2p8 at line 112 for ce
l1 sc1p3

Warning! sc2p8 latchlatch fanin 15 timing value = 0.0 for cell sc1p3 at
line 112
WhatDelayType: Warning! Unknown delay type sc2p8 at line 112 for ce
l1 sc1p3

Warning! sc2p8 hrflop fanin 15 timing value = 0.0 for cell sc1p3 at line
112
WhatDelayType: Warning! Unknown delay type sc2p8 at line 112 for ce
l1 sc1p3

Warning! sc2p8 gate fanin 16 timing value = 0.0 for cell sc1p3 at line 112
WhatDelayType: Warning! Unknown delay type sc2p8 at line 112 for ce
l1 sc1p3

Warning! sc2p8 latch fanin 16 timing value = 0.0 for cell sc1p3 at line
112
WhatDelayType: Warning! Unknown delay type sc2p8 at line 112 for ce
l1 sc1p3

Warning! sc2p8 flipflop fanin 16 timing value = 0.0 for cell sc1p3 at line
112
WhatDelayType: Warning! Unknown delay type sc2p8 at line 112 for ce
l1 sc1p3

Warning! sc2p8 latchlatch fanin 16 timing value = 0.0 for cell sc1p3 at
line 112
WhatDelayType: Warning! Unknown delay type sc2p8 at line 112 for ce
l1 sc1p3

Warning! sc2p8 hrflop fanin 16 timing value = 0.0 for cell sc1p3 at line
112
WhatDelayType: Warning! Unknown delay type sc2p8 at line 112 for ce
l1 sc1p3

Warning! sc2p8 gate fanin 17 timing value = 0.0 for cell sc1p3 at line 112
WhatDelayType: Warning! Unknown delay type sc2p8 at line 112 for ce
l1 sc1p3

Warning! sc2p8 latch fanin 17 timing value = 0.0 for cell sc1p3 at line
112
WhatDelayType: Warning! Unknown delay type sc2p8 at line 112 for ce
l1 sc1p3

Warning! sc2p8 flipflop fanin 17 timing value = 0.0 for cell sc1p3 at line
112
WhatDelayType: Warning! Unknown delay type sc2p8 at line 112 for ce
l1 sc1p3

Warning! sc2p8 latchlatch fanin 17 timing value = 0.0 for cell sc1p3 at
line 112
WhatDelayType: Warning! Unknown delay type sc2p8 at line 112 for ce
l1 sc1p3

Warning! sc2p8 hrflop fanin 17 timing value = 0.0 for cell sc1p3 at line
112 Reading pin cap values from
/n/auspex/s15/tbr/euterpe/proteus/leafgen/caps/cap.lib

.

From: Lisa Robinson [lisar@rhodan]
Sent: Friday, September 16, 1994 11:09 AM
To: 'dickson@rhodan'
Cc: 'veena@rhodan'; 'tbr@rhodan'; 'jeffm@rhodan'
Subject: branches

Rich,

Both bl and bul fail at the toplevel. (The tests pass on terp).

Let mew know if you need a dump.

Lisa R.

Design Name: z_euterpe_wrap
Run Date: 15994
Run ID: 6001

Using BOM:
Version BOM,v 119.0 1994/09/13 19:17:58 LT billz

Warning: Local BOM is out of date:

File: BOM Status: Needs Checkout

Version: 119.0 Tue Sep 13 21:26:48 1994
RCS Version: 119.8 /p/cvsroot/euterpe/verilog/bsrc/BOM,v
Sticky Tag: (none)
Sticky Date: (none)
Sticky Options: (none)

Simulator: z_euterpe_wrap.mif.mm was built on Tue Sep 13 22:36:44 1994

Run started on host: nosferatu at: Thu Sep 15 23:27:02 PDT 1994

b_be Ran ok
b_bne Ran ok
b_bl (in fail loop) Failed
b_bul (in fail loop) Failed
b_bge Ran ok
b_buge Ran ok
b_bande Ran ok
b_bandne Ran ok

.

From: tbr
Sent: Friday, September 16, 1994 11:38 AM
To: 'geert'; 'hopper'
Cc: 'vanthof'
Subject: Ignore last message
Follow Up Flag: Follow up
Flag Status: Red

Sorry, I was looking at the wrong log file. I don't think that particular problem has come back. However, I do have the following which is causing iteratnos to bomb:

Warning! clk_to_q gate fanin 1 timing value = 0.0 for cell xbhrdf8s at line 135706
Warning! clk_to_q flipflop fanin 1 timing value = 0.0 for cell xbhrdf8s at line 135717
Warning! clk_to_q latch fanin 1 timing value = 0.0 for cell xbhrdf8s at line 135718
Warning! clk_to_q hrflop fanin 1 timing value = 0.0 for cell xbhrdf8s at line 135739
Warning! clk_to_q gate fanin 1 timing value = 0.0 for cell xbhrdf16s at line 135798
Warning! clk_to_q flipflop fanin 1 timing value = 0.0 for cell xbhrdf16s at line 135809
Warning! clk_to_q latch fanin 1 timing value = 0.0 for cell xbhrdf16s at line 135810
Warning! clk_to_q hrflop fanin 1 timing value = 0.0 for cell xbhrdf16s at line 135831
Warning! clk_to_q gate fanin 1 timing value = 0.0 for cell xbhrdf24s at line 135844
Warning! clk_to_q flipflop fanin 1 timing value = 0.0 for cell xbhrdf24s at line 135855
Warning! clk_to_q latch fanin 1 timing value = 0.0 for cell xbhrdf24s at line 135856
Warning! clk_to_q hrflop fanin 1 timing value = 0.0 for cell xbhrdf24s at line 135877
Warning! clk_to_q gate fanin 1 timing value = 0.0 for cell xbhrdf32s at line 135890
Warning! clk_to_q flipflop fanin 1 timing value = 0.0 for cell xbhrdf32s at line 135901
Warning! clk_to_q latch fanin 1 timing value = 0.0 for cell xbhrdf32s at line 135902
Warning! clk_to_q hrflop fanin 1 timing value = 0.0 for cell xbhrdf32s at line 135923
Reading Cap/Delay table file /n/auspex/s15/tbr/euterpe/proteus/custom/time/tim.libWarning. Invalid format at line 10
ERROR! Cell cache at line 11 is not in legal cell list
Warning. Invalid format at line 15
ERROR! Cell cahalf at line 16 is not in legal cell list
Warning. Invalid format at line 17
ERROR! Cell cr at line 18 is not in legal cell list
Warning. Invalid format at line 23
ERROR! Cell ctag at line 24 is not in legal cell list
Warning. Invalid format at line 28
Warning. Invalid format at line 29
ERROR! Cell gtlb at line 30 is not in legal cell list
Warning. Invalid format at line 34
Warning. Invalid format at line 38
Warning. Invalid format at line 39
ERROR! Cell iosynchll at line 44 is not in legal cell list
Warning. Invalid format at line 45

(Dave we still seem to have one of those missing newlines!)

Tim

From: Richard Dickson [dickson@demeter]
Sent: Friday, September 16, 1994 3:53 PM
To: 'geert@demeter'; 'vanthof@demeter'
Subject: timing numbers

should i be worried about this stuff in my log file

Reading Cap/Delay table file
/n/rama/s5/dickson/euterpe/proteus/custom/tim
e/tim.libERROR! Cell cache at line 10 is not in legal cell list ERROR! Cell cahalf at
line 16 is not in legal cell list ERROR! Cell cr at line 19 is not in legal cell list
ERROR! Cell ctag at line 26 is not in legal cell list ERROR! Cell cxbbufdh12s at line 32
is not in legal cell list ERROR! Cell gt1b at line 34 is not in legal cell list ERROR!
Cell iobufdh4s at line 40 is not in legal cell list

dickson

From: vant [vanthof@hestia]
Sent: Friday, September 16, 1994 4:03 PM
To: 'Richard Dickson'
Cc: 'geert@demeter'; 'vanthof@demeter'; 'Bill Zuravleff'
Subject: Re: timing numbers

Richard Dickson writes:

```
>  
>  
>should i be worried about this stuff in my log file  
>  
>    Reading Cap/Delay table file  
>/n/rama/s5/dickson/euterpe/proteus/custom/tim  
>e/tim.libERROR! Cell cache at line 10 is not in legal cell list ERROR!  
>Cell cahalf at line 16 is not in legal cell list ERROR! Cell cr at  
>line 19 is not in legal cell list ERROR! Cell ctag at line 26 is not  
>in legal cell list ERROR! Cell cxbbufdh12s at line 32 is not in legal  
>cell list ERROR! Cell gt1b at line 34 is not in legal cell list ERROR!  
>Cell iobufdh4s at line 40 is not in legal cell list  
>  
>  
>                                dickson
```

I'm looking at this now. Topt will return with an exit code of 3 which will prevent the run from iterating past pass3.

I'm going to change topt so it will issue a warning which will allow you to continue.

Thanks,
Dave

--
Dave Van't Hof vanthof@microunity.com MicroUnity Systems Engineering,
Inc.
"What rolls down stairs, alone or in pairs, rolls over the neighbor's dog?"

What's great for a snack and fits on your back? It's log, log, log!"
LOG from BLAMMO! (tm) All kids love Log! #include
<std_disclaim.h>

.

From: tbr
Sent: Friday, September 16, 1994 9:53 PM
To: 'dickson'
Cc: 'billz'
Subject: forwarded message from Bill Zuravleff
Follow Up Flag: Follow up
Flag Status: Red

Can you hook these up please? I think these bits are comming from oct 6, 52:48.

----- Start of forwarded message -----

Return-Path: <billz@godzilla>
Received: from godzilla.microunity.com by gaea.microunity.com (4.1/muse1.3)
id AA09973; Fri, 16 Sep 94 19:07:55 PDT
Received: from localhost by godzilla.microunity.com (8.6.4/muse-sw.2)
id TAA20949; Fri, 16 Sep 1994 19:07:44 -0700
Message-Id: <199409170207.TAA20949@godzilla.microunity.com>
From: billz@godzilla (Bill Zuravleff)
To: doi@godzilla, lisar@godzilla, tbr@godzilla, tom@godzilla, chip@godzilla
Cc: euterpe-checkins-dist@godzilla
Subject: Release of BOMs by billz (euterpe)
Date: Fri, 16 Sep 1994 19:07:44 -0700

Checkin Message: -----

Have hooked up new-improved NB. Interface has changed.
Passes "pass1".
Cerberus bits remain unconnected. By all means, if you know
how to do this do so.

BOM Update in euterpe BOM 2.407
BOM Update in euterpe/verilog BOM 2.286
BOM Release in euterpe/verilog/bsrc BOM 122.0

----- End of forwarded message -----

.

From: Richard Dickson [dickson@demeter]
Sent: Friday, September 16, 1994 10:37 PM
To: 'billz@demeter'; 'tbr@demeter'
Subject: nb

bill,

i picked up your latest checkin of nb to see if i hacked cerberus and euterpe.V for addition of nb|plevel[4:0] and i was gmaking in nb and found that the first two plas in your pla src list bomded out. have you deleted these but because you have those files still laying around you dont see the error i'm seeing ?

dickson

.

From: Lisa Robinson [lisar@nosferatu]
Sent: Friday, September 16, 1994 11:14 PM
To: 'mws@nosferatu'; 'woody@nosferatu'; 'billz@nosferatu'
Cc: 'jeffm@nosferatu'; 'tbr@nosferatu'
Subject: store

I re-ran a bunch of tests against BOM 119 that had been rebuilt to take out the NOLOADSTORECONFLICT nops. The first to fail was store.

Dump is in /n/rhodan/s3/euterpe/verilog/bsrc/store.*

Lisa R.

.

From: Lisa Robinson [lisar@nosferatu]
Sent: Friday, September 16, 1994 11:26 PM
To: 'jeffm@nosferatu'
Cc: 'billz@nosferatu'; 'tbr@nosferatu'
Subject: dramharder

The trace of dramharder is in
/n/nosferatu/s2/euterpe/verilog/bsrc/res/16994.19623

Note that both drameasy and dram work on the zycad. Also (as we observed this afternoon) dramharder works okay in verilog.

Lisa R.

From: tbr
Sent: Saturday, September 17, 1994 11:57 AM
To: 'tom'
Cc: 'sysadmin'
Subject: disk space
Follow Up Flag: Follow up
Flag Status: Red

Has the new partiton been allocated for building stuff under
/u/chip/euterpe? I want to build a lot of stuff over the weekend.

Tim

.

From: Tom Laidig [tom@clio]
Sent: Saturday, September 17, 1994 12:54 PM
To: 'Tim B. Robinson'
Cc: 'tom@aphrodite'; 'sysadmin@aphrodite'
Subject: Re: disk space

Tim B. Robinson writes:

|
|Has the new partiton been allocated for building stuff under
|/u/chip/euterpe? I want to build a lot of stuff over the weekend.

Damn, I spaced that out yesterday!

Background for sysadmins, who probably haven't heard about this until now:

We're getting into the phase of development on euterpe where we need a bunch more disk space to hold the results of place/route runs on major subblocks of the chip. Experience suggests that this will require over 1GB of space, and it's highly desirable for this space to be backed up regularly and available efficiently over NFS. Tim asked me Thursday evening to prepare the necessary space on one of the new auspex disks after they came online. As mentioned above, I dropped the ball.

To get Tim running, I've appropriated s37 for this use. I hope this is OK -- if not I'll do whatever is needed to rearrange things more properly. Page me to get fastest response. Sorry to have done this unilaterally.

Tim:

The directory /n/auspex/s37/chip-euterpe-builds now exists and is owned by chip. As we discussed Thursday, you can su to chip and make subdirectories in this area with symlinks pointing to them. I told you wrong when I said you could pre-make the symlink and create the actual directory by mkdir'ing the symlink name -- this works to create files, but not directories. If you're stuck for how to name the actual subdirectories of this new area, I'd suggest names like 'mc-gards' for the subdirectory accessed from the euterpe/verilog/bsrc/mc/gards symlink.

--

Tom L

.

From: tbr
Sent: Saturday, September 17, 1994 1:03 PM
To: 'Tom Laidig'
Cc: 'sysadmin@aphrodite'; 'tom@aphrodite'
Subject: Re: disk space
Follow Up Flag: Follow up
Flag Status: Red

Tom Laidig wrote (on Sat Sep 17):

Tim B. Robinson writes:

|
|Has the new partiton been allocated for building stuff under
|/u/chip/euterpe? I want to build a lot of stuff over the weekend.

Damn, I spaced that out yesterday!

Background for sysadmins, who probably haven't heard about this until now:

We're getting into the phase of development on euterpe where we need a bunch more disk space to hold the results of place/route runs on major subblocks of the chip. Experience suggests that this will require over 1GB of space, and it's highly desirable for this space to be backed up regularly and available efficiently over NFS. Tim asked me Thursday evening to prepare the necessary space on one of the new auspex disks after they came online. As mentioned above, I dropped the ball.

To get Tim running, I've appropriated s37 for this use. I hope this is OK -- if not I'll do whatever is needed to rearrange things more properly. Page me to get fastest response. Sorry to have done this unilaterally.

Tim:

The directory /n/auspex/s37/chip-euterpe-builds now exists and is owned by chip. As we discussed Thursday, you can su to chip and make subdirectories in this area with symlinks pointing to them. I told you wrong when I said you could pre-make the symlink and create the actual directory by mkdir'ing the symlink name -- this works to create files, but not directories. If you're stuck for how to name the actual subdirectories of this new area, I'd suggest names like 'mc-gards' for the subdirectory accessed from the euterpe/verilog/bsrc/mc/gards symlink.

Thanks a lot tom. I have some stuff running locally, and as soon as that succeeds I'll set things up to run in the new space.

Tim

.

From: Eric Murray [ericm@MicroUnity.com]
Sent: Saturday, September 17, 1994 3:20 PM
To: 'Tom Laidig'
Cc: 'tbr@MicroUnity.com'; 'tom@MicroUnity.com'; 'sysadmin@MicroUnity.com'
Subject: Re: disk space

Tom Laidig wrote:

>
> Tim B. Robinson writes:
> |
> |Has the new partiton been allocated for building stuff under
> |/u/chip/euterpe? I want to build a lot of stuff over the weekend.
> |
> |Damn, I spaced that out yesterday!
> |
> |Background for sysadmins, who probably haven't heard about this until
> |now:
> |
> | We're getting into the phase of development on euterpe where we
> | need a bunch more disk space to hold the results of place/route
> | runs on major subblocks of the chip. Experience suggests that this
> | will require over 1GB of space, and it's highly desirable for this
> | space to be backed up regularly and available efficiently over
> | NFS. Tim asked me Thursday evening to prepare the necessary space
> | on one of the new auspex disks after they came online. As
> | mentioned above, I dropped the ball.
> |
> | To get Tim running, I've appropriated s37 for this use. I hope
> | this is OK -- if not I'll do whatever is needed to rearrange things
> | more properly. Page me to get fastest response. Sorry to have done
> | this unilaterally.

no problem. i'd still like to consolidate some of the existing
directories so we can free up one of the existing disks
for stuff like this that requires a full disk.

we also need to get the new disks onto a backup schedule. ken?

--
ericm ericm@microunity.com

.

From: tbr
Sent: Saturday, September 17, 1994 4:25 PM
To: 'Eric Murray'
Subject: Re: pager log message
Follow Up Flag: Follow up
Flag Status: Red

Eric Murray wrote (on Sat Sep 17):

Tim B. Robinson wrote:
>
> the sysadmin on call at this time is ericm
> page from tbr to ericm:
> 338 4152 cannot log into ghidra, says out of ptys but looks idle. tbr

it looks fine to me. maybe it was some transient problem.

Indeed it has let me in now. However, for 10 mins or so I was getting the same refusal and I still don't seem to be able to get 'domachine' to put up an xterm. When I rlogin in I get:

```
tbr@gamorra ~/euterpe/verilog/bsrc/cdio 407 % rlogin ghidra
Last login: Sat Feb 19 08:15:26 from tbrhds
SunOS Release 4.1.3 (MUSE_WS_WORKS) #16: Thu Mar 24 16:24:17 PST 1994
Can't open perl script "/usr/ucb/quota": Permission denied
```

Tim

.

From: tbr
Sent: Saturday, September 17, 1994 5:50 PM
To: 'vanthof'
Cc: 'geert'
Subject: topt bus error
Follow Up Flag: Follow up
Flag Status: Red

I have been trying to get a top level netlist again and I just got a bus error from topt. It did not make a core file. Here's the tail of the log:

IntrinsicWarning: Warning! No settop_to_q flipflop fanin 1 delay for gate xbmaj3dh8s
IntrinsicWarning: Warning! No usable intrinsic flipflop fanin 1 delay for gate xbxor3dh2s
NOTE: Cell xbxor3dh2s using 'intrinsic delay + .7RC' calculations.
IntrinsicWarning: Warning! No clk_to_q hrflop fanin 1 delay for flipflop sc1p8
NOTE: Cell sc1p8 using 'intrinsic delay + .7RC' calculations.
IntrinsicWarning: Warning! No clk_to_q flipflop fanin 1 delay for gate sccgdr
NOTE: Cell sccgdr using 'intrinsic delay + .7RC' calculations.

NOTE: Only the first 10000 ERRORS out of 12634 bad paths listed in the stat file
Use the -J option to increase this number

ERROR! 12634 paths exceeded cycle time. Check status file.
DC Load Calculations
/bin/sh: 20199 Bus error
make: *** [tbr_euterpe-pass1.strength] Error 138

Is it possible the bad data it triggering the problem?

Tim

From: Tim B. Robinson [tbr@aphrodite]
Sent: Saturday, September 17, 1994 5:50 PM
To: 'vanthof@aphrodite'
Cc: 'geert@aphrodite'
Subject: topt bus error

I have been trying to get a top level netlist again and I just got a bus error from topt. It did not make a core file. Here's the tail of the log:

```
IntrinsicWarning: Warning! No settop_to_q flipflop fanin 1 delay for gate xbmaj3dh8s
IntrinsicWarning: Warning! No usable intrinsic flipflop fanin 1 delay for gate xbxor3dh2s
NOTE: Cell xbxor3dh2s using 'intrinsic delay + .7RC' calculations.
IntrinsicWarning: Warning! No clk_to_q hrflop fanin 1 delay for flipflop
scip8
NOTE: Cell scip8 using 'intrinsic delay + .7RC' calculations.
IntrinsicWarning: Warning! No clk_to_q flipflop fanin 1 delay for gate sccgdr
NOTE: Cell sccgdr using 'intrinsic delay + .7RC' calculations.
```

NOTE: Only the first 10000 ERRORS out of 12634 bad paths listed in the stat file

Use the -J option to increase this number

ERROR! 12634 paths exceeded cycle time. Check status file.

DC Load Calculations

/bin/sh: 20199 Bus error

make: *** [tbr_euterpe-pass1.strength] Error 138

Is it possible the bad data is triggering the problem?

Tim

From: vant [vanthof@hestia]
Sent: Saturday, September 17, 1994 7:39 PM
To: 'Tim B. Robinson'
Cc: 'vanthof@aphrodite'; 'geert@aphrodite'
Subject: Re: topt bus error

Tim B. Robinson writes:

```
>  
>  
>I have been trying to get a top level netlist again and I just got a  
>bus error from topt. It did not make a core file. Here's the tail of  
>the log:  
>  
>IntrinsicWarning: Warning! No settop_to_q flipflop fanin 1 delay for  
gate xbmaj3dh8s  
>IntrinsicWarning: Warning! No usable intrinsic flipflop fanin 1 delay  
for gate xbxor3dh2s  
>NOTE: Cell xbxor3dh2s using 'intrinsic delay + .7RC' calculations.  
>IntrinsicWarning: Warning! No clk_to_q hrflop fanin 1 delay for  
>flipflop  
sc1p8  
>NOTE: Cell sc1p8 using 'intrinsic delay + .7RC' calculations.  
>IntrinsicWarning: Warning! No clk_to_q flipflop fanin 1 delay for gate  
sccgdr  
>NOTE: Cell sccgdr using 'intrinsic delay + .7RC' calculations.  
>  
>NOTE: Only the first 10000 ERRORS out of 12634 bad paths listed in the  
stat file  
> Use the -J option to increase this number  
>  
> ERROR! 12634 paths exceeded cycle time. Check status file.  
> DC Load Calculations  
>/bin/sh: 20199 Bus error  
>make: *** [tbr_euterpe-pass1.strength] Error 138  
>  
>  
>Is it possible the bad data it triggering the problem?  
>  
>Tim  
>
```

Sorry for the delay. We had an open house and we needed to be out of the house while it was going on.

Bad data should never cause a bus error... I'll look into it and fix it.

Thanks,
Dave

--
Dave Van't Hof vanthof@microunity.com MicroUnity Systems Engineering,
Inc.
"What rolls down stairs, alone or in pairs, rolls over the neighbor's dog?"

What's great for a snack and fits on your back? It's log, log, log!"
LOG from BLAMMO! (tm) All kids love Log! #include
<std_disclaim.h>

.

From: tbr
Sent: Saturday, September 17, 1994 8:10 PM
To: 'vant'
Cc: 'geert@aphrodite'; 'vanthof@aphrodite'
Subject: Re: Bogus warnings?
Follow Up Flag: Follow up
Flag Status: Red

vant wrote (on Sat Sep 17):

Tim B. Robinson writes:

>
>
>I'm now seeing zillions of messages of the form
>
>Warning! Instance xlu/G_ctrldata/G_db_7a/G_q_7a_123/p1p_1 (scsdm8) has strength of 0
>Warning! Instance xlu/G_ctrldata/G_db_7a/G_q_7a_124/p2p_1 (scsmf1) has strength of 0
>Warning! Instance xlu/G_ctrldata/G_db_7a/G_q_7a_124/p3p_1 (scsmf1) has strength of 0
>Warning! Instance xlu/G_ctrldata/G_db_7a/G_q_7a_124/p4p_1 (scsmf1) has strength of 0
>Warning! Instance xlu/G_ctrldata/G_db_7a/G_q_7a_124/p1p_1 (scsdm8) has strength of 0
>Warning! Instance xlu/G_ctrldata/G_db_7a/G_q_7a_125/p2p_1 (scsmf1) has strength of 0
>Warning! Instance xlu/G_ctrldata/G_db_7a/G_q_7a_125/p3p_1 (scsmf1) has strength of 0
>
>Given these are no longer supposed to be in the legal cell list,
>should I be getting these warnings?
>
>Tim
>

Yes. Topt gets the strength settings for cells from the legal cell list. If it's removed from the list, then the power level is set to '0'. Then, when topt reads in a strength file from a previous run, it gives a warning to let you know that the strength is set to 0.

I can change topt to only flag the cell type as being set to 0 once instead of each instance. This would significantly reduce the number of warnings you are seeing.

My intent was to warn of potential problems when it sees a 0 for a strength, but since we have lots of cells not on the legal cell list, this produces lots of senseless warnings.

Reducing it to one per type would be good. There really are zillions right now. I spoke too soon in the aearlier message. No bus error, but:

Warning! No PADOUT_ABM pin capacitance data for ttl3vnew
Disgorging Potentially BAD edif due to Errors edif file tbr_euterpe-pass1.edif.tmp
Writing edif structure: tbr_95_euterpe_45_pass1_46_edif_46_tmp
Memory usage: 162.778MB
Exit code: 4 (Bad Edif)

I'll look in the log file.

Tim

From: Tim B. Robinson [tbr@aphrodite]
Sent: Saturday, September 17, 1994 8:10 PM
To: 'vant'
Cc: 'geert@aphrodite'; 'vanthof@aphrodite'
Subject: Re: Bogus warnings?

vant wrote (on Sat Sep 17):

Tim B. Robinson writes:

```
>  
>  
>I'm now seeing zillions of messages of the form  
>  
>Warning! Instance xlu/G_ctrldata/G_db_7a/G_q_7a_123/plp_1 (scsdms) has strength of 0  
>Warning! Instance xlu/G_ctrldata/G_db_7a/G_q_7a_124/p2p_1 (scsmf1) has strength of 0  
>Warning! Instance xlu/G_ctrldata/G_db_7a/G_q_7a_124/p3p_1 (scsmf1) has strength of 0  
>Warning! Instance xlu/G_ctrldata/G_db_7a/G_q_7a_124/p4p_1 (scsmf1) has strength of 0  
>Warning! Instance xlu/G_ctrldata/G_db_7a/G_q_7a_124/p1p_1 (scsdms) has strength of 0  
>Warning! Instance xlu/G_ctrldata/G_db_7a/G_q_7a_125/p2p_1 (scsmf1) has strength of 0  
>Warning! Instance xlu/G_ctrldata/G_db_7a/G_q_7a_125/p3p_1 (scsmf1) has strength of 0  
>  
>Given these are no longer supposed to be in the legal cell list,  
>should I be getting these warnings?  
>  
>Tim  
>
```

Yes. Topt gets the strength settings for cells from the legal cell list. If it's removed from the list, then the power level is set to '0'. Then, when topt reads in a strength file from a previous run, it gives a warning to let you know that the strength is set to 0.

I can change topt to only flag the cell type as being set to 0 once instead of each instance. This would significantly reduce the number of warnings you are seeing.

My intent was to warn of potential problems when it sees a 0 for a strength, but since we have lots of cells not on the legal cell list, this produces lots of senseless warnings.

Reducing it to one per type would be good. There really are zillions right now. I spoke too soon in the earlier message. No bus error, but:

```
Warning! No PADOUT ABM pin capacitance data for ttl3vnew  
Disgorging Potentially BAD edif due to Errors edif file tbr_euterpe-pass1.edif.tmp  
Writing edif structure: tbr_95_euterpe_45_pass1_46_edif_46_tmp  
Memory usage: 162.778MB  
Exit code: 4 (Bad Edif)
```

I'll look in the log file.

Tim

.

From: Jay Tomlinson [woody@demeter]
Sent: Saturday, September 17, 1994 10:50 PM
To: 'Mark Semmelmeier'; 'Bill Zuravleff'
Cc: 'tbr@demeter'
Subject: Re: things for CD read miss

Mark Semmelmeier wrote (on Sat Sep 17):

> va: I will send r1 l r12 since I already have it staged that way for the exception
> address .
>
> dtag pa (padirty): I will add an R12.
>
> This is all that I have commented as needing R12. Do you also need an R12 dirty
> bit?
>
> Comments?
> Jay
>

thanks for giving this a go. what would you recommend on the
tag output staging (CTIOD vs. LT). also be warned that the tag
output is labelled R9 going into ctiod, goes through a reg,
but is still called R9 coming out (see euterpe.V).

Whoa! When did this happen? When I first started looking into LT I was told that
I would be receiving an R9 ctag, which agreed with the \$PIPE schematic. It looks
to me like I am actually receiving an R5 (R2 adr to ctiod, R3R4 adr to ctd, R5
data out of ctiod). When did the tag read move? It seems like this puts the tag
read at the same time as the data read. Are you trying to cover the tag with the
same load/store conflict logic? Staging a 58 bit tag is very expensive, even
more so in the area that LT lives (no routing available).

This is a big time dis-connect. Good thing this was noticed now.

It seems from a placement standpoint that ctiod would be the correct place. That
way if LT moves to make the floorplan fit, that is one less piece to move. Of
course, if that is done, that pretty much shoots down any possibility of using
the ctio block for the I-tag (beyond just copying the verilog). Since the
'ctioi' would work off a different signal than the 'cb4' than the d-side uses,
ctio may not work anyway (currently I think I can use it, just connect up this
other control to the cb4 interface, but until mws designs this I won't know for sure).

Bottom line, given the existing floorplan, it really doesn't matter which block
does the staging. I will add it to LT which leaves open the possibility that
ctio can be used for the I side.

Jay

.

From: vant [vanthof@hestia]
Sent: Saturday, September 17, 1994 11:27 PM
To: 'Tim B. Robinson'
Cc: 'vanthof@aphrodite'
Subject: Re: bad edif

Tim B. Robinson writes:

>
>
>I found the following in the log file. Far from clear what cells it's
>complaining about:
>
>Warning! Instance pll1 (pl_euh) has strength of 0
>Warning! Instance clk (cgclockbias) has strength of 0
>Warning! Instance tsensa (tsensa) has strength of 0
>Warning! Instance bgknobgen (bgknobgen) has strength of 0
>Warning! Instance bgproca2d (bgproca2d) has strength of 0
>ERROR! No 1C version of the phi_a2p3c port
>ERROR! No 1C version of the phi_b2p3c port
>ERROR! No 1C version of the phi_a2p3c port
>ERROR! No 1C version of the phi_b2p3c port
>Warning! Instance ci (cache) has strength of 0
>Warning! Instance cd (cache) has strength of 0
>Warning! Instance cti (ctag) has strength of 0
>Warning! Instance ctd (ctag) has strength of 0
>

I was wondering what module you were running when you got these errors.
I could not find any log file in your euterpe/verilog/bsrc/gards directory
which matched these.

Thanks,
Dave

--
Dave Van't Hof vanthof@microunity.com MicroUnity Systems Engineering, Inc.
"What rolls down stairs, alone or in pairs, rolls over the neighbor's dog?
What's great for a snack and fits on your back? It's log, log, log!"
LOG from BLAMMO! (tm) All kids love Log! #include <std_disclaim.h>

.

From: tbr
Sent: Saturday, September 17, 1994 11:32 PM
To: 'vant'
Cc: 'vanthof@aphrodite'
Subject: Re: bad edif
Follow Up Flag: Follow up
Flag Status: Red

vant wrote (on Sat Sep 17):

Tim B. Robinson writes:

>
>

>I found the following in the log file. Far from clear what cells it's
>complaining about:

>

>Warning! Instance pll1 (pl_euh) has strength of 0
>Warning! Instance clk (cgclockbias) has strength of 0
>Warning! Instance tsensa (tsensa) has strength of 0
>Warning! Instance bgknobgen (bgknobgen) has strength of 0
>Warning! Instance bgproca2d (bgproca2d) has strength of 0
>ERROR! No 1C version of the phi_a2p3c port
>ERROR! No 1C version of the phi_b2p3c port
>ERROR! No 1C version of the phi_a2p3c port
>ERROR! No 1C version of the phi_b2p3c port
>Warning! Instance ci (cache) has strength of 0
>Warning! Instance cd (cache) has strength of 0
>Warning! Instance cti (ctag) has strength of 0
>Warning! Instance ctd (ctag) has strength of 0
>

I was wondering what module you were running when you got these errors.
I could not find any log file in your euterpe/verilog/bsrc/gards directory
which matched these.

Trick question!

I was making the top level LVS netlist (or trying to). The rule that
converts the strength file to the edif file for some reason does not
write a log file. You can find it though in bsrc/makerrr.

Tim

.

From: tbr
Sent: Saturday, September 17, 1994 11:39 PM
To: 'vanthof'
Subject: another missing newline!
Follow Up Flag: Follow up
Flag Status: Red

Reading Cap/Delay table file /n/auspex/s15/tbr/euterpe/proteus/custom/time/tim.lib Warning! Cell cache at line 4 is not in legal cell list
Warning! Cell cahalf at line 10 is not in legal cell list

.

From: vant [vanthof@hestia]
Sent: Saturday, September 17, 1994 11:56 PM
To: 'Tim B. Robinson'
Cc: 'vanthof@aphrodite'
Subject: Re: another missing newline!

Tim B. Robinson writes:

>
>
> Reading Cap/Delay table file /n/auspex/s15/tbr/euterpe/proteus/custom/time/tim.libWarning! Cell cache at line 4 is not
in legal cell list
>Warning! Cell cahalf at line 10 is not in legal cell list
>
>

Thanks. I'll fix it.
Dave

--
Dave Van't Hof vanthof@microunity.com MicroUnity Systems Engineering, Inc.
"What rolls down stairs, alone or in pairs, rolls over the neighbor's dog?
What's great for a snack and fits on your back? It's log, log, log!"
LOG from BLAMMO! (tm) All kids love Log! #include <std_disclaim.h>

.

From: tbr
Sent: Sunday, September 18, 1994 12:17 AM
To: 'vanthof'
Subject: log file funny
Follow Up Flag: Follow up
Flag Status: Red

I note in the log file something odd about it reading in the intrinsic delays. There is a blank line, and it does not seem to report reading the custom and leafgen data (though I'm sure it must be):

ReadLegalCellFile: Warning! No atoms info for iobyte

Performing Edif Transformations...

Reading DC Loads file /n/auspex/s15/tbr/euterpe/proteus/leafgen/dclload/dclload.lib

Reading DC Loads file /n/auspex/s15/tbr/euterpe/proteus/exlax/dclload/dclload.lib

Reading DC Loads file /n/auspex/s15/tbr/euterpe/proteus/custom/dclload/dclload.lib

Reading LPE extracted data from hc-base.netcap.

Reading intrinsic delays from /n/auspex/s15/tbr/euterpe/proteus/exlax/time/tim.lib

Reading pin cap values from /n/auspex/s15/tbr/euterpe/proteus/leafgen/caps/cap.lib

Reading pin cap values from /n/auspex/s15/tbr/euterpe/proteus/exlax/caps/cap.lib

Reading pin cap values from /n/auspex/s15/tbr/euterpe/proteus/custom/caps/cap.lib

Status information in gards/hc-final.stat

.

From: tbr
Sent: Sunday, September 18, 1994 12:24 AM
To: 'lisar'
Subject: forwarded message from Mark Semmelmeyer
Follow Up Flag: Follow up
Flag Status: Red

Micro-arch may need updating

----- Start of forwarded message -----

Return-Path: <mws@ghidra>
Received: from ghidra.microunity.com by gaea.microunity.com (4.1/muse1.3)
id AA01488; Sat, 17 Sep 94 22:22:38 PDT
Received: from localhost by ghidra.microunity.com (8.6.4/muse-sw.2)
id WAA21674; Sat, 17 Sep 1994 22:22:04 -0700
Message-Id: <199409180522.WAA21674@ghidra.microunity.com>
From: mws@ghidra (Mark Semmelmeyer)
To: euterpe-checkins-dist@ghidra, lisar@ghidra, tbr@ghidra, tom@ghidra
Subject: euterpe/verilog/bsrc/ce ceregcore.V
Date: Sat, 17 Sep 1994 22:22:04 -0700

Update of /p/cvsroot/euterpe/verilog/bsrc/ce
In directory ghidra:/N/auspex/root/s24/mws/euterpe/verilog/bsrc/ce

Modified Files:
ceregcore.V

Log Message:
ce/ceregcore.V: Changed nbpllevel default from 0 to 16.

----- End of forwarded message -----

.

From: tbr
Sent: Sunday, September 18, 1994 12:49 AM
To: 'doi'
Subject: chipq interlocks
Follow Up Flag: Follow up
Flag Status: Red

I'm a bit worried we seemed to have two .checkoutrc's runnign to gether here, one in a subdir of the other. Isn't this supposed to be forbidden by default?

chipq

	ID	Target Directory	Machine(pid)	Who	Stat
1	280	euterpe/verilog/bsrc	staypuft(1906)	mws	0:09
2	281	euterpe/verilog/bsrc/hc	rhodan(23805)	tbr	0:01

Tim

From: vant [vanthof@hestia]
Sent: Sunday, September 18, 1994 2:15 PM
To: 'Tim B. Robinson'
Cc: 'Dave Van't Hof'; 'Geert Rosseel'; 'Mark Hofmann'
Subject: Re: More bad data?

Tim B. Robinson writes:

```
>
>vant wrote (on Sun Sep 18):
>
>   Tim B. Robinson writes:
>   >
>   >vant wrote (on Sat Sep 17):
>   >
>   >   Tim B. Robinson writes:
>   >   >
>   >   >
>   >   >IntrinsicWarning: Warning! No usable intrinsic flipflop fanin 1
delay for gate xbxor3dh8s
>   >   >NOTE: Cell xbxor3dh8s using 'intrinsic delay + .7RC'
calculations.
>   >   >IntrinsicWarning: Warning! No usable intrinsic flipflop fanin 1
delay for gate xbxor3dh3s
>   >   >NOTE: Cell xbxor3dh3s using 'intrinsic delay + .7RC'
calculations.
>   >   >IntrinsicWarning: Warning! No usable intrinsic flipflop fanin 1
delay for gate xbxor3dh4s
>   >   >NOTE: Cell xbxor3dh4s using 'intrinsic delay + .7RC'
calculations.
>   >   >
>   >   >
>   >   > I'm not so sure it's bad data. Let me look at this cuz when I
look at the
>   >   > delay tables, I believe all the data is there.
>   >   >
>   >   >Actually of course these are 3 level gates, probably with the same
>   >   >problem as the maj gates we noted before.
>   >   >
>   >   >Tim
>   >   >
>   >
>   > Well, I found and fixed the problem with the above errors, but
>   > others
have
>   > cropped up that were hidden.
>   >
>   > I'm heading off to bed and will work on this when I wake up.
>   >
>Sounds like a plan! Thanks for the help.
>
>Tim
>
```

Well, I found the problem in topt. My latest run on euterpe did not flag any of the above errors, but it did flag some missing data for the xbxor2dh6s cell for fanin 5 for top_to_g which is actually real missing data.

I've added support for the 'custom' setting in topt, but the effect is really no different from what topt was doing, except when reading in strength files. Which means that the scioff cell will still not get the extra clocks removed.

I filled my disk when running the euterpe test and topt didn't complain at all. I don't check for any sort of return code when writing the log file or stat file. This I will

change for the next release.

The list of cells with 0 strength should be much smaller when reading the the strength files. A cell will only be listed once.

Fixed a minor reporting funny (missing newline).

I'm sure I made other changes, but I've forgotten them, sorry.

I've left the previous version of topt as topt.old. I don't know if anyone is still using the 'really old' topt as topt.old or not. If someone is, then I'll move the topt.old over to topt.old.old like I used to do. However, if you run into problems, then use the topt.old, although it too has problems.

I will be out the rest of the afternoon as we have more people inspecting the house and we are heading over the hill to capitola for an art and wine festival. If there are problems please page me, and I'll work on the problems when I get back.

Thanks,
Dave

--

Dave Van't Hof vanthof@microunity.com MicroUnity Systems Engineering,
Inc.

"What rolls down stairs, alone or in pairs, rolls over the neighbor's dog?"

What's great for a snack and fits on your back? It's log, log, log!"

LOG from BLAMMO! (tm) All kids love Log! #include

<std_disclaim.h>

From: vant [vanthof@hestia]
Sent: Sunday, September 18, 1994 2:23 PM
To: 'Tim B. Robinson'; 'Geert Rosseel'
Cc: 'Dave Van't Hof'; 'Mark Hofmann'
Subject: bad topt

Spoke too soon. That version of topt I just installed completely barfed on euterpe. I don't know why.
I've reverted the topt back to the previous version.

Sorry. I'll try to fix it quickly.
Dave
--

Dave Van't Hof vanthof@microunity.com MicroUnity Systems Engineering,
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"What rolls down stairs, alone or in pairs, rolls over the neighbor's dog?"

What's great for a snack and fits on your back? It's log, log, log!"
LOG from BLAMMO! (tm) All kids love Log! #include
<std_disclaim.h>

From: vant [vanthof@hestia]
Sent: Sunday, September 18, 1994 2:31 PM
To: 'Geert Rosseel'; 'Tim B. Robinson'
Cc: 'Dave Van't Hof'; 'Mark Hofmann'
Subject: bad topt (fwd) fixed

vant writes:

>
>Spoke too soon. That version of topt I just installed completely
>barfed on euterpe. I don't know why.
>I've reverted the topt back to the previous version.
>
>Sorry. I'll try to fix it quickly.
>Dave

Found and fixed it. I had inverted the state when checking for custom cells in the legal cell list thus making all cells custom so topt did nothing.

Am I having fun yet? Oh boy.

I've started another releasebom and it should be done in a few minutes.
Thanks,
Dave

--
Dave Van't Hof vanthof@microunity.com MicroUnity Systems Engineering,
Inc.
"What rolls down stairs, alone or in pairs, rolls over the neighbor's dog?"
What's great for a snack and fits on your back? It's log, log, log!"
LOG from BLAMMO! (tm) All kids love Log! #include
<std_disclaim.h>

From: vant [vanthof@hestia]
Sent: Monday, September 19, 1994 11:29 AM
To: 'Orlando Hernando'; 'Mike Wageman'
Cc: 'Dave Van't Hof'; 'Mark Hofmann'; 'Geert Rosseel'; 'Fred Obermeier'
Subject: orchistmp upper drcs finished

Hi guys. The upper drc's finished for orchistmp. They are in

/u/vanthof/compass/mobi/orchis/tapeout/orchistmp_upper.err

you must be using the snapshot to look at these errors. If you get a chance to look at these, it would help a lot. If you need help locating the layouts, please let me know.

Thanks,
Dave

--
Dave Van't Hof vanthof@microunity.com MicroUnity Systems Engineering,
Inc.
"What rolls down stairs, alone or in pairs, rolls over the neighbor's dog?"
What's great for a snack and fits on your back? It's log, log, log!"
LOG from BLAMMO! (tm) All kids love Log! #include
<std_disclaim.h>

.

From: tbr
Sent: Monday, September 19, 1994 3:30 PM
To: 'vant'
Cc: 'Geert Rosseel'; 'Mark Hofmann'; 'Dave Van't Hof'
Subject: Re: More bad data?
Follow Up Flag: Follow up
Flag Status: Red

vant wrote (on Sun Sep 18):

Well, I found the problem in topt. My latest run on euterpe did not flag any of the above errors, but it did flag some missing data for the xbxor2dh6s cell for fanin 5 for top_to_q which is actually real missing data.

I've added support for the 'custom' setting in topt, but the effect is really no different from what topt was doing, except when reading in strength files. Which means that the scioff cell will still not get the extra clocks removed.

Thanks dave. I'm just back to running again and things look fine so far.

Tim

.

From: tbr
Sent: Monday, September 19, 1994 3:32 PM
To: 'Tom Laidig'
Subject: Re: X dixplay
Follow Up Flag: Follow up
Flag Status: Red

Tom Laidig wrote (on Mon Sep 19):

Tim B. Robinson writes:

| Where is the official X display for builds in chip that need to run
| gards?

The official display is iapetus:0. However, I haven't found it to be particularly reliable, and have resorted to using my own machine for all leafinold runs.

OK, well expect to see a few euterpe runs appear now and again!

What's the cause of the unreliability?

Tim

.

From: Tom Laidig [tom@clio]
Sent: Monday, September 19, 1994 5:12 PM
To: 'Tim B. Robinson'
Cc: 'Thomas Laidig'
Subject: Re: X dixplay

Tim B. Robinson writes:

Tom Laidig wrote (on Mon Sep 19):

Tim B. Robinson writes:

Where is the official X display for builds in chip that need to run
gards?

The official display is iapetus:0. However, I haven't found it to be
particularly reliable, and have resorted to using my own machine for all
leafmold runs.

OK, well expect to see a few euterpe runs appear now and again!

Oh, goody! At least they're probably sufficiently long-running that I
can shove the window to the background, unlike leafmold builds.

What's the cause of the unreliability?

I dunno. It seems that, after I've fired off a few leaf cells using
that X display, it gets hung. If I then try to connect to it in any
way (like saying ``xset -display iapetus:0 -q") my process hangs
forever.

--

Tom L

.

From: Derek Iverson [doi@demeter]
Sent: Monday, September 19, 1994 5:41 PM
To: 'tom@demeter'; 'tbr@demeter'
Subject: proteus/calliope/euterpe incompat in chipq.cf

I seem to remember us having incompat definitions in the chipq.cf file that listed incompatibilities between proteus/calliope and proteus/euterpe. In any event, the current chipq.cf file does not have any.

Anyone care to suggest some?

doi

From: Loretta Guarino [guarino@MicroUnity.com]
Sent: Monday, September 19, 1994 6:59 PM
To: 'lisa@MicroUnity.com'
Cc: 'vandyke@MicroUnity.com'; 'gmo@MicroUnity.com'
Subject: communications and predefined symbols

Sorry about the ambiguity in my notes!

Although it wasn't part of your original proposal, I understand that the predefined symbols without underscores were removed in the new compiler. Since you had changed the source, this didn't break the build, but did confuse some of the developers who were using the old symbols.

Most people didn't get a message that we were proceeding with the proposed changes and so it caught them off-guard. Someone (you? Don? Gmo? me?) should have sent mail about this change, much as Guillermo did for the software tools and simulator changes to new opcodes and for the new versions of the gnu-tools. I think we are pretty careful about doing this when we know the changes will impact developers. We still ought to alert people when we think we've taken care of the impact, just in case we miss anything.

Of course, I've still left "someone" unbound in the paragraph above...

Loretta

----- Forwarded Message

Return-Path: <lisa@MicroUnity.com>
Received: from calliope.microunity.com by gaea.microunity.com
(4.1/musel.3)
id AA02445; Mon, 19 Sep 94 16:44:29 PDT
Received: by calliope.microunity.com (931110.SGI/930416.SGI)
for guarino@gaea.microunity.com id AA26965; Mon, 19 Sep 94
16:44:28 -0700
Date: Mon, 19 Sep 94 16:44:28 -0700
From: lisa@MicroUnity.com (Lisa Repka)
Message-Id: <9409192344.AA26965@calliope.microunity.com>
To: Loretta Guarino <guarino@MicroUnity.com>
Subject: Re: Sept. 19 benchmark meeting
Cc: gmo@MicroUnity.com

> 1) The compiler's predefined symbols changed, per Lisa Repka's
> proposal. However, few people received any warning when this actually
> happened, which caused a certain amount of confusion. We need better
> communication about these sorts of events.

My apologies for any confusion. However, I'd like to point out that my proposal was simply to add some new pre-defines, not to change any existing ones. The only *change* I was proposing was the *usage*, and I did most of that myself (in all places I could think to in our currently checked-in sources) and I checked things in with fairly obvious comments, which should have been noticed by anybody who uses those files.

What's confusing *me* is the comment "We need better communication about these sorts of events." I can't imagine doing anything differently than I did--am I missing something?

lisa

----- End of Forwarded Message

From: Tim B. Robinson [tbr@aphrodite]
Sent: Monday, September 19, 1994 9:42 PM
To: 'euterpe@aphrodite'
Subject: xbhr cells

We have run into a problem with loading and timing related to the xbhr (half rate flop) cells. Here are some thoughts, but before we rush off changing anything I'd like to invite comments so we don't introduce worse problems than we need to fix already.

First the loading issue which I think is straight forward. We had a choice in the implementation of the xbhr cells to save a couple of atoms at the expense of significantly increased loading on the tau signal. We chose to do that, which does not seem to be a problem for the lower powered cells and gives us best atom utilization. However, in the higher powered cells (which are huge anyway), the saving is minimal (hopefully we won't have huge numbers of them), but the loading becomes so great that even our most powerful emitter follower buffer (24s) can only fannout to 5 or 6 of them and meet the loading rules. I thus propose that we change the implementation of the higher powered cells (say 12s and above) to include the extra couple of atoms to buffer off this loading. No changes to the euterpe source netlist would be needed.

Second for the timing. Currently, topt assumes that only hr-hr paths are eligible for double cycle timing. An hr to regular flop may be, but that can only be determined algorithmically. The net effect of this is that in a typical pipeline of these cells, the last stage always has to pay the cost of an hr (and the associated tau fannout buffers) but still has to make single cycle timing. A proposal would be to change topt's algorithm to allow double timing on any net driven by an hr, and change the logic model for this cell so the output is only valid in the second cycle after it is loaded (putting out X in the intervening cycle). If we pass logic verification we can be sure nothing is relying on the data being available in the first clock even with our unit delay simulation environment. Now it is expected that there are places in the current design, where to deal with the fact that hr to flop only ever gets 1 cycle, one extra stage of hr has been added (where a flop would have done), and where as a result we have created a situation where we rely on the data in the first cycle. It would be important to consider if we know all these places, so that on making the proposed change we would not waste a lot of time debugging errors which were introduced.

Finally, there would be cases (write enables to the custom arrays) where it would not be acceptable to deliver X half of the time. These instances would have to be replaced by explicit flosps with feedback.

Comments please . . .

Tim

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From: tbe@MicroUnity.com
Sent: Monday, September 19, 1994 9:44 PM
To: 'hestia'
Cc: 'pmayer'
Subject: minutes/actions from 9/19 pcb meeting

Following are minutes and action items from today's pcb meeting:

1) Main pcb split: issue of moving the dc-dc to the ac-dc pcb to eliminate risk of Hipot failures (immediate or latent) in low voltage components. Wayne discussed concern with manufacturing defects causing failures during production startup. Decision taken not to change current design for first 50 (nondeliverable) units, so as not to impact schedule or product cost.

action: tbe to revive investigation of high-current power bussing from early days of Hestia for contingency of changing design to isolate high voltage stuff in the future. This should be complete with a preliminary design by the time the first protos are built.

action: Wayne wants to analyze the implications of dc-dc on main pcb for Hipot test and possibly come up with additional tests to mitigate risk of damage.

2) The main pcb will require break-away edge tabs for manufacturing fixture requirements (TAB OLB, solder reflow machines, etc).

action: tbe to incorporate into next revision of criteria drawing.

3) Wayne asked for vias on HC bus between Calliope and Euterpe.

action: tbe to get minimum via spacing to wayne for evaluation wrt ICT.

action: tbe to verify with Hadco manufacturability of via array.

action: tbe to revise spacer cutout to maximize area for via fanout

4) Jay mentioned that the smart card connector is not shown on the mainpcb criteria.

action: tbe to incorporate into next revision. Patty can place where convenient for time being.

If I missed anything, please jump in!

-Tom

Tom Eich
MicroUnity Systems Engineering, Inc.
255 Caspian Dr. Sunnyvale, CA 94089
(408)734-8100, (408)734-8136 fax

tbe@microunity.com

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From: tbr
Sent: Monday, September 19, 1994 9:53 PM
To: 'Derek Iverson'
Cc: 'tom@demeter'
Subject: proteus/calliope/euterpe incompat in chipq.cf
Follow Up Flag: Follow up
Flag Status: Red

Derek Iverson wrote (on Mon Sep 19):

I seem to remember us having incompat definitions in the chipq.cf file that listed incompatibilities between proteus/calliope and proteus/euterpe. In any event, the current chipq.cf file does not have any.

Anyone care to suggest some?

We should have the same set related to dcells/bseplate/gards/ and clockbias at least.

Tim

From: Tim B. Robinson [tbr@aphrodite]
Sent: Monday, September 19, 1994 9:55 PM
To: 'Kurt Wampler'
Cc: 'agc@thoas'; 'billz@thoas'; 'dickson@thoas'; 'geert@thoas'; 'hopper@thoas'; 'ong@thoas'; 'tom@thoas'; 'vo@thoas'
Subject: export_subblock support

Kurt Wampler wrote (on Mon Sep 19):

Upon request, I've added support for SOFA sub-blocks to be able to export themselves as a single cell, which may subsequently be used in other place & route work. Here's what I changed:

```
proteus/Makefile.defs
  Added definitions for "gasavepins" program
```

```
proteus/Makefile.rules
  Added "gasavepins" step to the formula for making the ".dff" file.
```

```
proteus/misc/gards.cvp
  Added code to activate the delay obstructions (category 15) generated
  by the gasavepins step so that targets on one-pin nets at the sub-block
  level will be protected against internal routing that might obstruct
  these targets.
```

```
euterpe/verilog/bsrc/Makefile.share
  Added a rule to make gards/%.pdl & gards/%.obs by invoking the shell
  script "export_subblock".
```

```
euterpe/verilog/bsrc/export_subblock
  This script derives a PDL file and an OBS file for the subblock, once it
  has been routed to a converged solution. The PDL and OBS files are copied
  into ${CHIPROOT}/gards/subblocks, where they can be consumed by other
  place & route problems.
```

NOTE: In order to get the placement obstruction information for one of these sub-blocks, it is necessary to add a little bit of code to your gplace batch control file (gplace.nic). Using "cdio" as an example:

```
readobs cdio.obs
actobst; use; ok
```

I think this file gets built each time by a cat in the Makefile.
If so, it will need fixing there.

If I've corrupted anything in the process of making these changes, please let me know.

- Kurt

.

From: Lisa Robinson [lisar@nosferatu]
Sent: Monday, September 19, 1994 11:49 PM
To: 'woody@nosferatu'; 'jeffm@nosferatu'
Cc: 'mws@nosferatu'; 'billz@nosferatu'; 'tbr@nosferatu'
Subject: gtlbaccess1

Dump in /n/rhodan/s3/euterpe/verilog/bsrc/gtlbaccess1.*

Lisa R.

From: Mark Hofmann [hopper@boreas]
Sent: Tuesday, September 20, 1994 12:04 AM
To: 'Tim B. Robinson'
Cc: 'euterpe@aphrodite'
Subject: Re: xbhr cells

Tim B. Robinson writes:

We have run into a problem with loading and timing related to the xbhr (half rate flop) cells. Here are some thoughts, but before we rush off changing anything I'd like to invite comments so we don't introduce worse problems than we need to fix already.

First the loading issue which I think is straight forward. We had a choice in the implementation of the xbhr cells to save a couple of atoms at the expense of significantly increased loading on the tau signal. We chose to do that, which does not seem to be a problem for the lower powered cells and gives us best atom utilization. However, in the higher powered cells (which are huge anyway), the saving is minimal (hopefully we won't have huge numbers of them), but the loading becomes so great that even our most powerful emitter follower buffer (24s) can only fannout to 5 or 6 of them and meet the loading rules. I thus propose that we change the implementation of the higher powered cells (say 12s and above) to include the extra couple of atoms to buffer off this loading. No changes to the euterpe source netlist would be needed.

Unless these bigger cells turn out to be a problem to build (and I think they ought to be easier, routing wise) it seems clear that we should adopt this approach.

Second for the timing. Currently, topt assumes that only hr-hr paths are eligible for double cycle timing. An hr to regular flop may be, but that can only be determined algorithmically. The net effect of this is that in a typical pipeline of these cells, the last stage always has to pay the cost of an hr (and the associated tau fannout buffers) but still has to make single cycle timing. A proposal would be to change topt's algorithm to allow double timing on any net driven by an hr, and change the logic model for this cell so the output is only valid in the second cycle after it is loaded (putting out X in the intervening cycle). If we pass logic verification we can be sure nothing is relying on the data being available in the first clock even with our unit delay simulation environment. Now it is expected that there are places in the current design, where to deal with the fact that hr to flop only ever gets 1 cycle, one extra stage of hr has been added (where a flop would have done), and where as a result we have created a situation where we rely on the data in the first cycle. It would be important to consider if we know all these places, so that on making the proposed change we would not waste a lot of time debugging errors which were introduced.

So Topt would always double time hr -> ff paths? Or would we want a switch to tel Topt explicitly which paths to double time and, default, single time such paths? This, latter, would be the conservative thing. We could time in the default mode initially. If we get timing violations in the hr -> ff paths then examine these and if X in the first cycle is okay add something to the (power.tab.local) file to let Topt know to double time this particular path.

Finally, there would be cases (write enables to the custom arrays) where it would not be acceptable to deliver X half of the time. These instances would have to be replaced by explicit flops with feedback.

Comments please . . .
Tim

-hopper

.

From: tbr
Sent: Tuesday, September 20, 1994 12:07 AM
To: 'Mark Hofmann'
Cc: 'euterpe@aphrodite'
Subject: Re: xbhr cells
Follow Up Flag: Follow up
Flag Status: Red

Mark Hofmann wrote (on Mon Sep 19):

So Topt would always double time hr -> ff paths? Or would we want a switch to tel Topt explicitly which paths to double time and, default, single time such paths? This, latter, would be the conservative thing. We could time in the default mode intially. If we get timing violations in the hr -> ff paths then examine these and if X in the first cycle is okay add something to the (power.tab.local) file to let Topt know to double time this particular path.

We could do it this way, but I think it's the case that any single cycle paths we have are caused by having to make the last cell in the chain an hr to prevent the previous segment being single cycle. The main thing is to be sure the simulation enviornment is conservative enough no mistake can slip through.

Tim

From: Tim B. Robinson [tbr@aphrodite]
Sent: Tuesday, September 20, 1994 12:07 AM
To: 'Mark Hofmann'
Cc: 'euterpe@aphrodite'
Subject: Re: xbhr cells

Mark Hofmann wrote (on Mon Sep 19):

So Topt would always double time hr -> ff paths? Or would we want a switch to tel Topt explicitly which paths to double time and, default, single time such paths? This, latter, would be the conservative thing. We could time in the default mode initially. If we get timing violations in the hr -> ff paths then examine these and if X in the first cycle is okay add something to the (power.tab.local) file to let Topt know to double time this particular path.

We could do it this way, but I think it's the case that any single cycle paths we have are caused by having to make the last cell in the chain an hr to prevent the previous segment being single cycle.
The main thing is to be sure the simulation environment is conservative enough no mistake can slip through.

Tim

.

From: Lisa Robinson [lisar@nosferatu]
Sent: Tuesday, September 20, 1994 12:13 AM
To: 'jeffm@nosferatu'
Cc: 'mws@nosferatu'; 'woody@nosferatu'; 'billz@nosferatu'; 'tbr@nosferatu'
Subject: exaligneasay

New dump in /n/rhodan/s3/euterpe/verilog/bsrc/exaliagneasy.*

Lisa R.

From: Mark Semmelmeier [mws@demeter]
Sent: Tuesday, September 20, 1994 2:47 AM
To: 'Mark Hofmann'
Cc: 'euterpe@demeter'
Subject: Re: xbhr cells

hopper writes:

> So Topt would _always_ double time hr -> ff paths? Or would we want a
switch
> to tel Topt explicitly which paths to double time and, default, single
> time such paths? This, latter, would be the conservative thing. We
> could time in the default mode intially. If we get timing violations
> in the hr -> ff paths then examine these and if X in the first cycle
> is okay add something to the (power.tab.local) file to let Topt know
> to double time this particular path.

For such a switch to be useful, we would have to be able to specify the path by source and destination to handle one part sourcing or receiving both 1 and 2 tick paths. For example, although one intuitive specification might be to let the source be tagged as a 1 or 2 tick path driver, it if were uniformly 1 tick then we would just change it into a flop (I am assuming flop vs hr would no longer affect the number of ticks in the incoming paths to the source part in this example). What kind of power.tab.local somethings did you have in mind? Regular expressions? (Or are they too slow?)

mws

From: Mark Hofmann [hopper@cyclops]
Sent: Tuesday, September 20, 1994 5:36 AM
To: 'hardheads@cyclops'
Subject: Database updates

Hi,

In order to minimize the number of restarts we're going to batch our changes to the various proteus/euterpe timing, cap, dclload, pdl, layout, etc., etc. files. We settled on making these updates twice a day- at 10am and at 5pm. We started a bit late today, and still have one job remaking pdl in proteus/gards running (do a "chipq"- it's job ID 337). When that finishes we'll be done with the 10am release.

-thanks,
hopper

From: Mark Hofmann [hopper@boreas]
Sent: Tuesday, September 20, 1994 8:49 AM
To: 'Mark Semmelmeier'
Cc: 'euterpe@demeter'
Subject: Re: xbhr cells

Mark Semmelmeier writes:

For such a switch to be useful, we would have to be able to specify the path by source and destination to handle one part sourcing or receiving both 1 and 2 tick paths. For example, although one intuitive specification might be to let the source be tagged as a 1 or 2 tick path driver, it if were uniformly 1 tick then we would just change it into a flop (I am assuming flop vs hr would no longer affect the number of ticks in the incoming paths to the source part in this example). What kind of power.tab.local somethings did you have in mind? Regular expressions? (Or are they too slow?)

I had something very simple in mind. Just the exact source and destination. I wanted to make it both easy for Topt and explicit to the user and designer so it would be clear just which paths were affected.

-hopper

From: Tom Laidig [tom@clio]
Sent: Tuesday, September 20, 1994 10:03 AM
To: 'Bill Zuravleff'
Cc: 'hopper@boreas'; 'mws@demeter'; 'euterpe@demeter'
Subject: Re: xbhr cells

Bill Zuravleff writes:

tbr, mws and hopper write:

...we would have to be able
to specify the path by source and destination to handle
one part sourcing or receiving both 1 and 2 tick paths.

In addition to being useful (required?) for topt, this info would be
useful in the hdl netlist in order to determine which model of hr --
one whose output is good only after
2 ticks or one whose output is good after both one and two ticks -- to
use to detect an algorithmic dependency on a one cycle path.

I don't understand how we can verify the functionality of such a system. If topt is told
by some auxilliary file that some paths are 1-tick and others are 2-tick, how can we get
verilog to understand this?

I think I like tbr's original suggestion much better: define, for the purposes of both
verilog and topt, that xbhr cells take 2 ticks to produce a result. If some xbhr cell's
output is used after 1 tick, then replace it with an explicit muxff cell. Verilog will
tell us if we miss any of these.

--

Tom L

.

From: tbr
Sent: Tuesday, September 20, 1994 11:05 AM
To: 'Mark Hofmann'
Cc: 'euterpe@demeter'; 'Mark Semmelmeier'
Subject: Re: xbhr cells
Follow Up Flag: Follow up
Flag Status: Red

Mark Hofmann wrote (on Tue Sep 20):

Mark Semmelmeier writes:

For such a switch to be useful, we would have to be able to specify the path by source and destination to handle one part sourcing or receiving both 1 and 2 tick paths.

For example, although one intuitive specification might be to let the source be tagged as a 1 or 2 tick path driver, it if were uniformly 1 tick then we would just change it into a flop (I am assuming flop vs hr would no longer affect the number of ticks in the incoming paths to the source part in this example).

What kind of power.tab.local somethings did you have in mind? Regular expressions? (Or are they too slow?)

I had something very simple in mind. Just the exact source and destination. I wanted to make it both easy for Topt and explicit to the user and designer so it would be clear just which paths were affected.

I want something extremely simple too. We don't have time for complicated tweaking of every path.

Tim

From: Tim B. Robinson [tbr@aphrodite]
Sent: Tuesday, September 20, 1994 11:05 AM
To: 'Mark Hofmann'
Cc: 'euterpe@demeter'; 'Mark Semmelmeier'
Subject: Re: xbhr cells

Mark Hofmann wrote (on Tue Sep 20):

Mark Semmelmeier writes:

For such a switch to be useful, we would have to be able to specify the path by source and destination to handle one part sourcing or receiving both 1 and 2 tick paths. For example, although one intuitive specification might be to let the source be tagged as a 1 or 2 tick path driver, it if were uniformly 1 tick then we would just change it into a flop (I am assuming flop vs hr would no longer affect the number of ticks in the incoming paths to the source part in this example). What kind of power.tab.local somethings did you have in mind? Regular expressions? (Or are they too slow?)

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I want something extremely simple too. We don't have time for complicated tweaking of every path.

Tim

From: Tim B. Robinson [tbr@aphrodite]
Sent: Tuesday, September 20, 1994 11:15 AM
To: 'Bill Zuravleff'
Cc: 'euterpe@demeter'; 'hopper@boreas'; 'mws@demeter'
Subject: Re: xbhr cells

Bill Zuravleff wrote (on Tue Sep 20):

tbr, mws and hopper write:

...we would have to be able
to specify the path by source and destination to handle
one part sourcing or receiving both 1 and 2 tick paths.

In addition to being useful (required?) for topt, this
info would be useful in the hdl netlist in order to determine
which model of hr -- one whose output is good only after
2 ticks or one whose output is good after both one and
two ticks -- to use to detect an algorithmic
dependency on a one cycle path.

You can't do that, unless we double up on the physical cess too. The reason is that when
we come to simulate the LVS netlist there would be no indication of what is needed.

This whole situation is getting out of hand in my opinion. The reason for having these
things at all is to save area where we are staging along major busses at half rate. Using
them to save a few atoms here and there in control is a waste of time (of which we have
all too little). By spending so much time on details we are likely to lose more area in a
missed global optimization than we will save.

Tim

From: Buffalo Chip [chip@ghidra]
Sent: Tuesday, September 20, 1994 11:22 AM
To: 'geert@ghidra'
Subject: output of euterpe/verilog/bsrc/hc/.checkoutrc

Tue Sep 20 09:12:29 PDT 1994 (geert Tue, 20 Sep 1994 09:12:07 -0700)
euterpe/verilog/bsrc/hc
[Release BOM (V37.0) in euterpe/verilog/bsrc/hc (Tue Sep 20 09:12:29 PDT 1994)]

Dir euterpe/verilog/bsrc/hc BOM 37.0

```
-27.2 (genpim.pl)
35.1 .checkoutrc
1.19 Makefile
34.1 genpim0.pl
32.3 genpim1.pl
12.5 gentst.pl
1.26 hc.V
3.6 hc.h
8.5 hc.ut
17.1 hc_buf_8.V
6.1 hc_cmp6.V
27.5 hc_control.pim
8.7 hc_device.V
3.15 hc_driver.V
4.1 hc_error.Veqn
12.1 hc_fifo8.V
12.1 hc_fifo8ctrl.Veqn
3.10 hc_ostate.pla
3.2 hc_parse.Veqn
3.6 hc_prbctrl.pla
3.1 hc_rxcrc.Veqn
3.3 hc_sdecode.Veqn
3.7 hc_sid.Veqn
3.2 hc_tagmatch.V
3.2 hc_txrc.Veqn
13.1 hcinstantiate.h
27.2 pimlib.pl
17.3 power.tab.local
==> running euterpe/verilog/bsrc/hc/.checkoutrc (Tue Sep 20 09:12:36 PDT
1994) <==
#
# turn off pgroute
#
[ -f nopgroute ] || touch nopgroute
#
# use padtiles
#
[ -f usepadtiles ] || touch usepadtiles
#
# use pifpack
#
[ -f usepifpack ] || touch usepifpack
#
# insert an instance of the clock tree
#
[ -f addclock ] || touch addclock
#
# Disable old dcell placement obstruction # [ -f gards/noobs ] || touch gards/noobs # #
Now do it . . .
#
gmake GARDS_DISPLAY=clio:0.0 hc0-iter
gmake[1]: Entering directory
~/N/auspex/root/s10/chip/euterpe/verilog/bsrc/hc'
```

```

cat /n/auspex/s10/chip/euterpe/proteus/verilog/dxlib/xlib.config
/n/auspex/s10/chip/euterpe/proteus/verilog/dclib/clib.config
/n/auspex/s10/chip/euterpe/proteus/verilog/delib/elib.config > v2e.config
CHIPROOT=/n/auspex/s10/chip/euterpe
/n/auspex/s10/chip/euterpe/tools/bin/v2e -host staypuft -f vfiles -o hc0.v2e -y ../io -y
/n/auspex/s10/chip/euterpe/proteus/verilog/mlib
+libext+.v -y /n/auspex/s10/chip/euterpe/proteus/verilog/dxlib -y
/n/auspex/s10/chip/euterpe/proteus/verilog/dclib -y
/n/auspex/s10/chip/euterpe/proteus/verilog/delib
V2E 1.0a Sep 20, 1994 09:09:44
* Copyright Cadence Design Systems Inc. 1990. *
* All Rights Reserved. Licensed Software. *
* Confidential and proprietary information which is the *
* property of Cadence Design Systems Inc. *
Compiling source file "hc.v"
Compiling source file "hc_tagmatch.v"
Compiling source file "hc_cmp6.v"
Compiling source file "hc_fifo8.v"
Compiling source file "hc_buf_8.v"
Compiling source file "hc_ostate.v"
Compiling source file "hc_prbctrl.v"
Compiling source file "hc_sdecode.v"
Compiling source file "hc_txcrc.v"
Compiling source file "hc_sid.v"
Compiling source file "hc_parse.v"
Compiling source file "hc_rxcrc.v"
Compiling source file "hc_fifo8ctrl.v"
Compiling source file "hc_error.v"
Scanning library directory "../io"
Scanning library directory
"/n/auspex/s10/chip/euterpe/proteus/verilog/mlib"
Scanning library directory
"/n/auspex/s10/chip/euterpe/proteus/verilog/dxlib"
Scanning library directory
"/n/auspex/s10/chip/euterpe/proteus/verilog/dclib"
Warning! library directory
"/n/auspex/s10/chip/euterpe/proteus/verilog/delib" was specified but not needed.
Highest level modules:
hc

Reading configuration file v2e.config ....
Processing configuration file ....
Translating Verilog source ....
Writing output to hc0.v2e ....
0 warnings 0 errors
End of V2E 1.0a Sep 20, 1994 09:11:01
CHIPROOT=/n/auspex/s10/chip/euterpe
/n/auspex/s10/chip/euterpe/tools/bin/emerge -f -R -p emerge.tab -e hc0.v2e -o hc0.edif -O
hc0.emerge.log -I ../cg/cgclockbias.v2e cgclockbias

Running emerge compiled on Sun Sep 18 12:32:16 PDT 1994

Consuming edif file hc0.v2e
Found edif structure: HC0_46_V2E
Flattening edif;
flattened 1119 instances; created 1508 nets in HC0_46_V2E
Reading Edif file for instance placement: ../cg/cgclockbias.v2e
Consuming power table information file emerge.tab
Performing Edif Transformations...
Warning! Port PHI_A2P already top level.
Warning! Port PHI_B2P already top level.
Disgorging edif file hc0.edif
Writing edif structure: hc0_46_edif
Memory usage: 7.043MB
#
# Get an initial sdl file. A manhattan approximation will be used # gmake
GARDS_DISPLAY=clio:0.0 CYCLETIME=895 gards/hc0-pass2.sdl
gmake[2]: Entering directory

```



```

`/N/auspex/root/s10/chip/euterpe/verilog/bsrc/hc'
CHIPROOT=/n/auspex/s10/chip/euterpe
/n/auspex/s10/chip/euterpe/tools/bin/topt -p
/n/auspex/s10/chip/euterpe/proteus/misc/power.tab -p power.tab.local -h
/n/auspex/s10/chip/euterpe/proteus/leafgen/dclload/dclload.lib -h
/n/auspex/s10/chip/euterpe/proteus/exlax/dclload/dclload.lib -h
/n/auspex/s10/chip/euterpe/proteus/custom/dclload/dclload.lib -g
/n/auspex/s10/chip/euterpe/proteus/leafgen/toptList -g
/n/auspex/s10/chip/euterpe/proteus/exlax/toptList -g
/n/auspex/s10/chip/euterpe/proteus/custom/toptList \
-A /n/auspex/s10/chip/euterpe/proteus/leafgen/caps/cap.lib -A
/n/auspex/s10/chip/euterpe/proteus/exlax/caps/cap.lib -A
/n/auspex/s10/chip/euterpe/proteus/custom/caps/cap.lib \
-H /n/auspex/s10/chip/euterpe/proteus/leafgen/time/tim.lib -H
/n/auspex/s10/chip/euterpe/proteus/custom/time/tim.lib -d
/n/auspex/s10/chip/euterpe/proteus/exlax/time/tim.lib \
-l 895 \
-e hc0.edif \
-k hc0-pass1.strength -B gards/hc0-pass1.sdl -s gards/hc0-pass1.stat -O gards/hc0-
pass1.topt.log \
-z 2 -M mobimos -R -t 50 -b 10 -a 24 -0 -F

```

Running topt compiled on Sun Sep 18 19:32:36 GMT 1994

```

Processing a: Mobimos, Flop/Latch design
Consuming edif file hc0.edif
Found edif structure: hc0_46.edif
Flattening edif;
HC already flat.
found 1120 instances; found 2846 nets in hc0_46.edif
Consuming power table information file
/n/auspex/s10/chip/euterpe/proteus/misc/power.tab
Consuming power table information file power.tab.local
Reading Stats file
/n/auspex/s10/chip/euterpe/proteus/leafgen/stats.ec1
Reading Stats file
/n/auspex/s10/chip/euterpe/proteus/leafgen/stats.cmos
Reading Stats file /n/auspex/s10/chip/euterpe/proteus/exlax/stats.ea
Reading Stats file
/n/auspex/s10/chip/euterpe/proteus/custom/stats.ec1
Reading Legal Cell List file
/n/auspex/s10/chip/euterpe/proteus/leafgen/toptList
Reading Legal Cell List file
/n/auspex/s10/chip/euterpe/proteus/exlax/toptList
ReadLegalCellFile: Warning! No atoms info for ealnf36s9x4a
Reading Legal Cell List file
/n/auspex/s10/chip/euterpe/proteus/custom/toptList
Performing Edif Transformations...
Reading DC Loads file
/n/auspex/s10/chip/euterpe/proteus/leafgen/dclload/dclload.lib
Reading DC Loads file
/n/auspex/s10/chip/euterpe/proteus/exlax/dclload/dclload.lib
Reading DC Loads file
/n/auspex/s10/chip/euterpe/proteus/custom/dclload/dclload.lib
Reading intrinsic delays from
/n/auspex/s10/chip/euterpe/proteus/exlax/time/tim.lib

Reading pin cap values from
/n/auspex/s10/chip/euterpe/proteus/leafgen/caps/cap.lib
Reading pin cap values from
/n/auspex/s10/chip/euterpe/proteus/exlax/caps/cap.lib
Reading pin cap values from
/n/auspex/s10/chip/euterpe/proteus/custom/caps/cap.lib
Status information in gards/hc0-pass1.stat Warning! Cell cgclockbias not on legal
cell list.
Any gate in it's path is not AC power optimized
No swing calculations will be performed Warning! Cell scsynchll not on legal cell
list.

```

Any gate in it's path is not AC power optimized
No swing calculations will be performed
Pruning flattened network of unused instances... 31 pruned in 2
passes.

Checking/Setting swing values...

Found 16 Warnings! Please check stat file!

Reading Cap/Delay table file

/n/auspex/s10/chip/euterpe/proteus/leafgen/time/tim.lib

Reading Cap/Delay table file

/n/auspex/s10/chip/euterpe/proteus/custom/time/tim.lib

Warning! Cell cache at line 4 is not in legal cell list Warning! Cell cahalf at line 10
is not in legal cell list Warning! Cell cr at line 13 is not in legal cell list Warning!
Cell ctg at line 20 is not in legal cell list Warning! Cell gt1b at line 23 is not in
legal cell list Warning! Cell scggbf0 at line 52 is not in legal cell list Warning!
Cell scsof3v3 at line 188 is not in legal cell list

Connecting floating differential inputs to net vref_0ph...

Connected 0 inputs to net vref_0ph...

DC Load checks only for cell(s):

eawwlvref56s7x4a eawwlvref20s10x1a eawwlvref16s2x4a xbc01df32s
xbc01df24s xbc01df16s xbc01df12s xbc01df8s xbc01df6s xbc01df4s
xbc01df2s xbc01 dcbfmos2ecldf16s xbcmos2ecldf12s xbcmos2ecldf8s
xbcmos2ecldf4s xbcmos2ecldf2s xbcmos2ec1 Warning! No CKFI_AD1PH pin capacitance
data for cgclockbias Warning! No CKFI_BD1PH pin capacitance data for cgclockbias Warning!
No CKRI_AD1PH pin capacitance data for cgclockbias Warning! No CKRI_BD1PH pin capacitance
data for cgclockbias Warning! No CLR_ABM<8> pin capacitance data for cgclockbias Warning!
No CLR_ABM<7> pin capacitance data for cgclockbias Warning! No CLR_ABM<6> pin capacitance
data for cgclockbias Warning! No CLR_ABM<5> pin capacitance data for cgclockbias Warning!
No CLR_ABM<4> pin capacitance data for cgclockbias Warning! No CLR_ABM<3> pin capacitance
data for cgclockbias Warning! No CLR_ABM<2> pin capacitance data for cgclockbias Warning!
No CLR_ABM<1> pin capacitance data for cgclockbias Warning! No CLR_ABM<0> pin capacitance
data for cgclockbias Warning! No PHI_ANM<8> pin capacitance data for cgclockbias Warning!
No PHI_ANM<7> pin capacitance data for cgclockbias Warning! No PHI_ANM<6> pin capacitance
data for cgclockbias Warning! No PHI_ANM<5> pin capacitance data for cgclockbias Warning!
No PHI_ANM<4> pin capacitance data for cgclockbias Warning! No PHI_ANM<3> pin capacitance
data for cgclockbias Warning! No PHI_ANM<2> pin capacitance data for cgclockbias Warning!
No PHI_ANM<1> pin capacitance data for cgclockbias Warning! No PHI_ANM<0> pin capacitance
data for cgclockbias Warning! No PHI_BNM<8> pin capacitance data for cgclockbias Warning!
No PHI_BNM<7> pin capacitance data for cgclockbias Warning! No PHI_BNM<6> pin capacitance
data for cgclockbias Warning! No PHI_BNM<5> pin capacitance data for cgclockbias Warning!
No PHI_BNM<4> pin capacitance data for cgclockbias Warning! No PHI_BNM<3> pin capacitance
data for cgclockbias Warning! No PHI_BNM<2> pin capacitance data for cgclockbias Warning!
No PHI_BNM<1> pin capacitance data for cgclockbias Warning! No PHI_BNM<0> pin capacitance
data for cgclockbias Warning! No RD_BM<8> pin capacitance data for cgclockbias Warning!
No RD_BM<7> pin capacitance data for cgclockbias Warning! No RD_BM<6> pin capacitance
data for cgclockbias Warning! No RD_BM<5> pin capacitance data for cgclockbias Warning!
No RD_BM<4> pin capacitance data for cgclockbias Warning! No RD_BM<3> pin capacitance
data for cgclockbias Warning! No RD_BM<2> pin capacitance data for cgclockbias Warning!
No RD_BM<1> pin capacitance data for cgclockbias Warning! No RD_BM<0> pin capacitance
data for cgclockbias Warning! No SI_AM<8> pin capacitance data for cgclockbias Warning!
No SI_AM<7> pin capacitance data for cgclockbias Warning! No SI_AM<6> pin capacitance
data for cgclockbias Warning! No SI_AM<5> pin capacitance data for cgclockbias Warning!
No SI_AM<4> pin capacitance data for cgclockbias Warning! No SI_AM<3> pin capacitance
data for cgclockbias Warning! No SI_AM<2> pin capacitance data for cgclockbias Warning!
No SI_AM<1> pin capacitance data for cgclockbias Warning! No SI_AM<0> pin capacitance
data for cgclockbias Warning! No VFFMAX pin capacitance data for cgclockbias Warning! No
VFFMIN pin capacitance data for cgclockbias Warning! No VFFNOM pin capacitance data for
cgclockbias Warning! No VFFREFMAX pin capacitance data for cgclockbias Warning! No
VFFREFMIN pin capacitance data for cgclockbias Warning! No VFFREFNOM pin capacitance data
for cgclockbias Warning! No VFFREFVAR pin capacitance data for cgclockbias Warning! No
VFFVAR pin capacitance data for cgclockbias Warning! No VRRG<2> pin capacitance data for
cgclockbias Warning! No VRRG<1> pin capacitance data for cgclockbias Warning! No VRRG<0>
pin capacitance data for cgclockbias Warning! No XFER_BM<8> pin capacitance data for
cgclockbias Warning! No XFER_BM<7> pin capacitance data for cgclockbias Warning! No
XFER_BM<6> pin capacitance data for cgclockbias Warning! No XFER_BM<5> pin capacitance
data for cgclockbias Warning! No XFER_BM<4> pin capacitance data for cgclockbias Warning!
No XFER_BM<3> pin capacitance data for cgclockbias Warning! No XFER_BM<2> pin capacitance

data for cgclockbias Warning! No XFER_BM<1> pin capacitance data for cgclockbias Warning!
No XFER_BM<0> pin capacitance data for cgclockbias Warning! No PHI_A2P pin capacitance
data for scsynchl1 Warning! No PHI_B2P pin capacitance data for scsynchl1 Warning! No D0
_AD0PF pin capacitance data for scsynchl1 Warning! No D0_AND0PF pin capacitance data for
scsynchl1

Ignoring these nets:
PHI_B2P PHI_A2P vref_0ph

Optimizing power...

Iteration: 1
Path power optimizer
ERROR! 3 paths exceeded cycle time. Check status file.
DC Load Calculations
Unpowered Instance check: 11 found.
Iteration: 2
Path power optimizer
ERROR! 3 paths exceeded cycle time. Check status file.
DC Load Calculations
Unpowered Instance check: 10 found.
Iteration: 3
Path power optimizer
ERROR! 3 paths exceeded cycle time. Check status file.
DC Load Calculations
Unpowered Instance check: 10 found.

Squeezing out extra time in paths.

Iteration: 4
Path power optimizer
ERROR! 3 paths exceeded cycle time. Check status file.
DC Load Calculations
Unpowered Instance check: 10 found.
Iteration: 5
Path power optimizer
ERROR! 3 paths exceeded cycle time. Check status file.
DC Load Calculations
Unpowered Instance check: 10 found.
Iteration: 6
Path power optimizer
ERROR! 3 paths exceeded cycle time. Check status file.
DC Load Calculations
Unpowered Instance check: 10 found.

Savings by squeezing out extra time = (6063 - 6081) = -0.30% Change from original input
power = (6081 - 80) = 98.68%

Warning! 10 unpowered or untouched instances.

NOTE: 694 unpowered nets.

NOTE: 55 nets with delays less than 50.00ps

NOTE: Power levels changed for 1060 instances.

Atoms:	count	atom	bjt	isrc	pld	clock
BJT Totals:						
	1089	8946	19307	12595	12234	6228

Generating instance drive strength file hc0-pass1.strength

Disgorging sdl file gards/hc0-pass1.sdl

Writing sdl structure: hc0_46_edif

Memory usage: 26.402MB

Exit code would be 2 (Failed Max Timing), but is forced to 0

CHIPROOT=/n/auspex/s10/chip/euterpe

/n/auspex/s10/chip/euterpe/tools/bin/pdlcat -p

/n/auspex/s10/chip/euterpe/clockbias:/n/auspex/s10/chip/euterpe/gards/dcel

1:/n/auspex/s10/chip/euterpe/proteus/gards/leaf:/n/auspex/s10/chip/euterpe

/proteus/gards/sofa:/n/auspex/s10/chip/euterpe/proteus/gards/dcell `grep -v '^#' < hc0-

```

pass1.strength | awk '{print $4;}' | sort | uniq | awk '{printf ("%s.pdl ", $1)}'` >
gards/hc0-pass1macros.temp mv guards/hc0-pass1macros.temp guards/hc0-pass1macros.pdl
**** SLNET hc0-pass1
Tue Sep 20 09:16:49 PDT 1994
sed -e 's!DESIGN_NAME!hc0-pass1!' -e 's!EDIF_FILE!hc0-pass1.sdl!' -e 's!
CHIPROOT!/n/auspex/s10/chip/euterpe!' -e 's!TECH_GPLACE!gplace.mobi234!' -e 's!TECH_REDIR!
redit.mobi234!' < /n/auspex/s10/chip/euterpe/proteus/misc/guards.vrf > guards/hc0-pass1.vrf
echo "cd `abspath`/guards; \
echo translate_all | HOME=/n/auspex/s10/chip/euterpe/tools
LM_LICENSE_FILE=/n/auspex/s10/chip/euterpe/tools/sl/license/license.dat
DISPLAY=cli0:0.0 SL_TOTAL_DURATION=500 CHIPROOT=/n/auspex/s10/chip/euterpe
/n/auspex/s10/chip/euterpe/tools/sl/net/dir/slnet hc0-pass1" | /usr/local/bin/rexec
ghidra sh
** SLNET 1.037 ** SL_NET V1.000 -- Netlist Manipulator Copyright (c) 1993,1994 SILVAR-
LISCO. All rights reserved.
Design: hc0-pass1 Started at: 94/09/20 09:16:52

```

Loading file "hc0-pass1.sdl".

```

[XBC01DF12S]
[XBC01DF24S]
[XBCMOS2ECLDF2S]
[XBCMOS2ECLDF4S]
[XBBUFD16S]
[XBFFBDF32S]
[XBFFBDF24S]
[XBFFBDH12S]
[XBFFBDH24S]
[XBFFBDH3S]
[XBFFBDH4S]
[XBFFBDH16S]
[XBFFBDH2S]
[XBFFBDF2S]
[XBFFBDF4S]
[XBFFBDF6S]
[XBFFBDF8S]
[XBFFBDF32S]
[XBFFBDF12S]
[XBFFBDF16S]
[XBOR3DF6S]
[XBOR3DF8S]
[XBOR3DF4S]
[XBOR3DF2S]
[XBOR11DF4S]
[XBORFF5DF24S]
[XBORFF5DH6S]
[XBORFF5DH12S]
[XBORFF5DF32S]
[XBORFF5DF4S]
[XBORFF5DF8S]
[XBORFF2DH8S]
[XBORFF2DF2S]
[XBORFF2DF24S]
[XBORFF2DH4S]
[XBORFF2DH4S]
[XBORFF2DH16S]
[XBORFFB2DH16S]
[XBORFFB2DH24S]
[XBORFF2DH24S]
[XBORFF2DF12S]
[XBORFF2DF8S]
[XBORFF2DF4S]
[XBORFF2DF6S]
[XBMUXFF2DF12S]
[XBMUXFF2DF4S]
[XBMUXFFB2DH8S]
[XBMUXFF2DH12S]

```

[XBMUXFF2DF8S]
[XBMUXFF2DH2S]
[XBMUXFF2DH3S]
[XBMUXFF2DH4S]
[XBMUXFF2DH6S]
[XBOR4DF6S]
[XBOR4DF4S]
[XBOR4DF16S]
[XBOR4DF8S]
[XBOR4DF2S]
[XBOR5DF12S]
[XBOR5DF16S]
[XBOR5DF4S]
[XBOR5DF2S]
[XBOR5DF6S]
[XBOR5DF8S]
[XBOR6DF16S]
[XBOR6DF6S]
[XBOR6DF12S]
[XBOR6DF2S]
[XBOR6DF4S]
[XBOR7DF2S]
[XBOR7DF16S]
[XBOR7DF4S]
[XBOR7DF6S]
[XBOR8DF4S]
[XBOR8DF8S]
[XBOR8DF12S]
[XBOR8DF2S]
[XBOR9DF8S]
[XBOR9DF4S]
[XBOR10DF4S]
[XBOR2DF2S]
[XBOR2DF4S]
[XBORFFB3DH4S]
[XBORFF3DF12S]
[XBORFF3DF24S]
[XBORFF3DF32S]
[XBORFF3DH2S]
[XBORFF3DF6S]
[XBORFF3DF16S]
[XBORFF3DF8S]
[XBORFF3DF4S]
[XBORFF3DH8S]
[XBORFF7DF4S]
[XBORFF7DF12S]
[XBORFFB7DF12S]
[XBORFF7DF2S]
[XBORFF4DH6S]
[XBORFF4DF16S]
[XBORFF4DH2S]
[XBORFFB4DH24S]
[XBORFF4DF24S]
[XBORFF4DF6S]
[XBORFF9DH6S]
[XBORFF17DH6S]
[XBORFF6DH4S]
[XBORFF6DF6S]
[XBORFF6DF4S]
[XBORFF13DF24S]
[XBORFF11DF24S]
[XBORFF8DF24S]
[XBORFF8DF32S]
[XBMUXFF8DF4S]
[XBMUXFF8DH3S]
[XBOR2DF4S]
[XBMUXFF4DF4S]
[XBMUXFF4DH3S]

[XBMUXFF6DH24S]
[XBMUXFF9DF6S]
[XBMUXFF3DH24S]
[XBBUFDH2S]
[XBBUFDH16S]
[SCSYNCHLL]
[CGCLOCKBIAS]
[HC]

** Warning: No nets connected to component CGCLOCKBIAS.

Translating...

[XBC01DF12S]
[XBC01DF24S]
[XBCMOS2ECLDF2S]
[XBCMOS2ECLDF4S]
[XBBUFDH16S]
[XBFFBDF32S]
[XBFFDF24S]
[XBFFBDH12S]
[XBFFDH24S]
[XBFFDH3S]
[XBFFDH4S]
[XBFFDH16S]
[XBFFDH2S]
[XBFFDF2S]
[XBFFDF4S]
[XBFFDF6S]
[XBFFDF8S]
[XBFFDF32S]
[XBFFDF12S]
[XBFFDF16S]
[XBOR3DF6S]
[XBOR3DF8S]
[XBOR3DF4S]
[XBOR3DF2S]
[XBOR11DF4S]
[XBORFF5DF24S]
[XBORFF5DH6S]
[XBORFF5DH12S]
[XBORFF5DF32S]
[XBORFF5DF4S]
[XBORFF5DF8S]
[XBORFF2DH8S]
[XBORFF2DF2S]
[XBORFF2DF24S]
[XBORFFB2DH4S]
[XBORFF2DH4S]
[XBORFF2DH16S]
[XBORFFB2DH16S]
[XBORFFB2DH24S]
[XBORFF2DH24S]
[XBORFF2DF12S]
[XBORFF2DF8S]
[XBORFF2DF4S]
[XBORFF2DF6S]
[XBMUXFF2DF12S]
[XBMUXFF2DF4S]
[XBMUXFFB2DH8S]
[XBMUXFF2DH12S]
[XBMUXFF2DF8S]
[XBMUXFF2DH2S]
[XBMUXFF2DH3S]
[XBMUXFF2DH4S]
[XBMUXFF2DH6S]
[XBOR4DF6S]
[XBOR4DF4S]
[XBOR4DF16S]
[XBOR4DF8S]
[XBOR4DF2S]

[XBOR5DF12S]
[XBOR5DF16S]
[XBOR5DF4S]
[XBOR5DF2S]
[XBOR5DF6S]
[XBOR5DF8S]
[XBOR6DF16S]
[XBOR6DF6S]
[XBOR6DF12S]
[XBOR6DF2S]
[XBOR6DF4S]
[XBOR7DF2S]
[XBOR7DF16S]
[XBOR7DF4S]
[XBOR7DF6S]
[XBOR8DF4S]
[XBOR8DF8S]
[XBOR8DF12S]
[XBOR8DF2S]
[XBOR9DF8S]
[XBOR9DF4S]
[XBOR10DF4S]
[XBOR2DF2S]
[XBOR2DF4S]
[XBORFFB3DH4S]
[XBORFF3DF12S]
[XBORFF3DF24S]
[XBORFF3DF32S]
[XBORFF3DH2S]
[XBORFF3DF6S]
[XBORFF3DF16S]
[XBORFF3DF8S]
[XBORFF3DF4S]
[XBORFF3DH8S]
[XBORFF7DF4S]
[XBORFF7DF12S]
[XBORFFB7DF12S]
[XBORFF7DF2S]
[XBORFF4DH6S]
[XBORFF4DF16S]
[XBORFF4DH2S]
[XBORFFB4DH24S]
[XBORFF4DF24S]
[XBORFF4DF6S]
[XBORFF9DH6S]
[XBORFF17DH6S]
[XBORFF6DH4S]
[XBORFF6DF6S]
[XBORFF6DF4S]
[XBORFF13DF24S]
[XBORFF11DF24S]
[XBORFF8DF24S]
[XBORFF8DF32S]
[XBMUXFF8DF4S]
[XBMUXFF8DH3S]
[XBXOR2DF4S]
[XBMUXFF4DF4S]
[XBMUXFF4DH3S]
[XBMUXFF6DH24S]
[XBMUXFF9DF6S]
[XBMUXFF3DH24S]
[XBBUFD2S]
[XBBUFDH16S]
[SCSYNCHLL]
[CGCLOCKBIAS]
[HC]

Netlist Info :

```

-----
Number of logic types      : 123
Number of nets             : 2302
Number of components       : 1089
Number of component pins   : 10875
Number of pins/comp        : 9.986226
Number of nets/comp        : 2.113866

```

Size estimation :

```

-----
size | TYPE | # inst | size/inst | total
-----+-----+-----+-----+-----
| XBORFF2DF8S | 1 | 1 | 1
| XBMUXFFB2DH8S | 6 | 1 | 6
| XBOR3DF8S | 1 | 1 | 1
| XBOR5DF12S | 3 | 1 | 3
| XBOR8DF4S | 2 | 1 | 2
| XBOR6DF2S | 4 | 1 | 4
| XBORFFB2DH4S | 4 | 1 | 4
| XBORFF3DF16S | 3 | 1 | 3
| XBORFF17DH6S | 1 | 1 | 1
| XBORFF3DF4S | 3 | 1 | 3
| XBFFDF4S | 3 | 1 | 3
| XBOR10DF4S | 3 | 1 | 3
| XBOR3DF6S | 4 | 1 | 4
| XBCMOS2ECLDF4S | 16 | 1 | 16
| XBOR5DF8S | 2 | 1 | 2
| XBOR8DF2S | 1 | 1 | 1
| XBBUFD16S | 3 | 1 | 3
| XBORFF2DH4S | 6 | 1 | 6
| XBMUXFF2DF12S | 1 | 1 | 1
| XBFFDF6S | 5 | 1 | 5
| XBORFF5DF4S | 2 | 1 | 2
| XBOR5DF6S | 5 | 1 | 5
| XBMUXFF2DH6S | 3 | 1 | 3
| XBOR3DF4S | 22 | 1 | 22
| XBORFF2DF24S | 1 | 1 | 1
| XBORFF11DF24S | 2 | 1 | 2

```


XBOR4DF16S	3	1	3
XBORFF2DF6S	1	1	1
XBORFF2DH24S	1	1	1
XBMUXFF9DF6S	3	1	3
XBMUXFF2DF8S	3	1	3
XBFFBDF32S	1	1	1
XBFFDH24S	1	1	1
XBFFDH3S	9	1	9
XBFFDF8S	4	1	4
XBORFF7DF4S	1	1	1
XBORFF8DF32S	1	1	1
XBOR5DF4S	2	1	2
XBOR9DF8S	1	1	1
XBORFF3DF12S	3	1	3
XBOR3DF2S	54	1	54
SCSYNCHLL	9	1	9
XBOR7DF6S	2	1	2
XBORFF6DH4S	1	1	1
XBOR6DF16S	4	1	4
XBORFF13DF24S	4	1	4
XBORFFB7DF12S	1	1	1
XBBUFDH16S	2	1	2
XBORFF4DF24S	3	1	3
XBORFF4DF6S	15	1	15
XBORFF2DH8S	1	1	1
XBFFDF12S	9	1	9
XBORFF3DH2S	2	1	2
XBMUXFF2DH2S	200	1	200
XBOR7DF4S	4	1	4
XBOR2DF4S	48	1	48
XBOR5DF2S	9	1	9
XBORFF5DH6S	1	1	1
XBCMOS2ECLDF2S	4	1	4
XBORFFB2DH16S	1	1	1

XBORFF6DF6S	8	1	8
XBFFBDH12S	2	1	2
XBORFF3DF32S	1	1	1
XBORFF7DF2S	8	1	8
XBORFF2DF4S	30	1	30
XBFFDF16S	2	1	2
XBOR7DF2S	1	1	1
XBOR6DF12S	8	1	8
XBORFF7DF12S	1	1	1
XBORFF3DF8S	4	1	4
XBOR9DF4S	2	1	2
XBOR4DF8S	30	1	30
XBMUXFF2DF4S	4	1	4
XBORFFB3DH4S	1	1	1
XBORFF4DF16S	2	1	2
XBORFF8DF24S	2	1	2
XBBUFD2S	16	1	16
XBORFF9DH6S	1	1	1
XBFFDF24S	4	1	4
XBFFDH16S	4	1	4
XBFFDH2S	14	1	14
XBMUXFF6DH24S	9	1	9
XBORFF5DF32S	1	1	1
XBOR4DF6S	2	1	2
XBOR11DF4S	5	1	5
XBOR8DF12S	1	1	1
XBOR2DF4S	21	1	21
XBORFF5DF8S	1	1	1
XBC01DF12S	1	1	1
XBORFF5DH12S	1	1	1
CGCLOCKBIAS	1	1	1
XBORFF2DH16S	1	1	1
XBMUXFF4DF4S	8	1	8
XBMUXFF2DH3S	82	1	82

XBORFFB2DH24S	2	1	2
XBFFDF32S	7	1	7
XBORFF2DF2S	2	1	2
XBORFF6DF4S	1	1	1
XBOR6DF6S	2	1	2
XBOR8DF8S	1	1	1
XBOR4DF4S	3	1	3
XBORFF2DF12S	12	1	12
XBOR2DF2S	59	1	59
XBOR5DF16S	1	1	1
XBORFF3DF24S	1	1	1
XBORFFB4DH24S	1	1	1
XBORFF3DF6S	3	1	3
XBMUXFF2DH12S	6	1	6
XBMUXFF4DH3S	1	1	1
XBOR4DF2S	46	1	46
XBOR6DF4S	5	1	5
XBORFF4DH6S	11	1	11
XBC01DF24S	2	1	2
XBMUXFF8DF4S	8	1	8
XBOR7DF16S	1	1	1
XBORFF5DF24S	2	1	2
XBMUXFF8DH3S	7	1	7
XBMUXFF2DH4S	64	1	64
XBORFF3DH8S	1	1	1
XBFFDH4S	5	1	5
XBMUXFF3DH24S	32	1	32
XBORFF4DH2S	7	1	7
XBFFDF2S	2	1	2
+-----+-----+-----+			
TOTAL	1089	1	1089
+-----+-----+-----+			

Warning : No "SL_SIZE" attributes found on the cells!
Default size (1) was used for all cells.

To change this default add an attribute "SL_SIZE" to the cells.

```
slnet > 09:17:09 Terminating Normally on 94/09/20
Elapsed CPU time 00:00:15
Elapsed wall time 00:00:17
End of Program
```

Normal Termination ...

Tue Sep 20 09:17:09 PDT 1994

**** PCOMP hc0-pass1

Tue Sep 20 09:17:10 PDT 1994

```
sed -e 's!DESIGN_NAME!hc0-pass1!' -e 's!EDIF_FILE!hc0-pass1.sdl!' -e 's!
CHIPROOT!/n/auspex/s10/chip/euterpe!' -e 's!TECH_GPLACE!gplace.mobi234!' -e 's!TECH_REDIT!
redit.mobi234!' < /n/auspex/s10/chip/euterpe/proteus/misc/gards.vrf > guards/hc0-pass1.vrf
rm -f guards/hc0-pass1.dff (echo "cd `abspath`/guards; \
```

```
HOME=/n/auspex/s10/chip/euterpe/tools
```

```
LM LICENSE FILE=/n/auspex/s10/chip/euterpe/tools/sl/license/license.dat
DISPLAY=clio:0.0 SL_TOTAL_DURATION=500 CHIPROOT=/n/auspex/s10/chip/euterpe
/n/auspex/s10/chip/euterpe/tools/sl/bin/invoke pcomp hc0-pass1 -listing hc0-
pass1.pcomp.lis" | /usr/local/bin/rexec ghidra sh && sleep 10 && \
```

```
HOME=/n/auspex/s10/chip/euterpe/tools
```

```
LM LICENSE FILE=/n/auspex/s10/chip/euterpe/tools/sl/license/license.dat
DISPLAY=clio:0.0 SL_TOTAL_DURATION=500 CHIPROOT=/n/auspex/s10/chip/euterpe
/n/auspex/s10/chip/euterpe/tools/bin/gastatus -ds guards/hc0-pass1 ) || (mv guards/hc0-
pass1.pcomp.lis guards/hc0-pass1.pcomp.lis.ERROR; false)
```

Requires a minimum license of guardsfel_3 or guardsl_3 .

Applicable licenses available at your installation :

guardsconfig_3

Checked out one user token of a guardsconfig_3 license.

GARDS PCOMP 7.119 -- Physical Compiler

Copyright (c) 1994 SILVAR-LISCO. All rights reserved.

Design: hc0-pass1 Started at: 94/09/20 09:17:15

PCOMP Version 7.1.19 of April 29, 1994

Processing Logic description: HC

Processing Expansion level: SLNET

... Start of netlist processing.

... Circuit name: HC

... Processing CDL.

... CHIPNAME:SOFA;

... Processing header of user PDL.

... PHYSICALLIB:PBUILD;

... Processing header of system PDL.

... PHYSICALLIB:PBUILD;

... Processing rest of user PDL.

... Processing rest of system PDL.

... Processing TDL.

... TECHNOLOGYLIB:SOFA;

... Computed Grid Size = 1000

... Final Processing.

... Successful physical compilation (with warnings).

>>> Loading logical netlist.

... Successful completion. GARDS design file created.

Terminated at : 94/09/20 09:17:27

Elapsed CPU time : 0 Hrs 0 Mins 8 Secs

Elapsed wall clock time : 0 Hrs 0 Mins 12 Secs

Tue Sep 20 09:17:38 PDT 1994

HOME=/n/auspex/s10/chip/euterpe/tools

LM LICENSE FILE=/n/auspex/s10/chip/euterpe/tools/sl/license/license.dat

DISPLAY=clio:0.0 SL_TOTAL_DURATION=500 CHIPROOT=/n/auspex/s10/chip/euterpe

```

/n/auspex/s10/chip/euterpe/tools/bin/pim2pif hc0-pass1.pim -xrf gards/hc0-pass1.xrf -dff
gards/hc0-pass1.dff -noHole \
-obstructionPdl /n/auspex/s10/chip/euterpe/gards/sofa/sofa.pdl \
-obstructionCdl /n/auspex/s10/chip/euterpe/gards/sofa/sofa.cdl \
-libraryPdl gards/hc0-pass1macros.pdl -ecl -tech mobi -sdl \

/n/auspex/s10/chip/euterpe/tools/bin/pim2pif: Preparing input files...
/n/auspex/s10/chip/euterpe/tools/bin/pim2pif: Reading
/n/auspex/s10/chip/euterpe/gards/sofa/sofa.pdl...
/n/auspex/s10/chip/euterpe/tools/bin/pim2pif: Reading gards/hc0-pass1.dff...
/n/auspex/s10/chip/euterpe/tools/bin/pim2pif: Fetching bounding box from
/n/auspex/s10/chip/euterpe/gards/sofa/sofa.cdl...
/n/auspex/s10/chip/euterpe/tools/bin/pim2pif: Checking
/n/auspex/s10/chip/euterpe/gards/sofa/sofa.cdl for fixed obstructions...
/n/auspex/s10/chip/euterpe/tools/bin/pim2pif: Checking
/n/auspex/s10/chip/euterpe/gards/sofa/sofa.cdl for Ecl obstructions...
cat: write error: Broken pipe
/n/auspex/s10/chip/euterpe/tools/bin/pim2pif: Processing the hc0-pass1.pim file...
/n/auspex/s10/chip/euterpe/tools/bin/pim2pif.ex: 52 rows (52 non-empty) ...spanning 28
columns (28 maximum cells/row) ...for a total of 1088 cells were written to `hc0-
pass1.pim.pif.0'.
/n/auspex/s10/chip/euterpe/tools/bin/pim2pif.ex: (1914, 491) to (2344,
653) [215 by 54 ECL atoms]
/n/auspex/s10/chip/euterpe/tools/bin/pim2pif.ex: 8946 ECL atoms placed in 11610 [-430
obstructions] atom area [80.02% dense]
/n/auspex/s10/chip/euterpe/tools/bin/pim2pif.ex: WARNING: Potential errors, check warnings
file `hc0-pass1.pim.warn'
#pim2pif.ex Version 0.2.14 Tue Sep 13 17:03:51 PDT 1994 mv hc0-pass1.pim.warn gards
HOME=/n/auspex/s10/chip/euterpe/tools
LM_LICENSE_FILE=/n/auspex/s10/chip/euterpe/tools/sl/license/license.dat
DISPLAY=clio:0.0 SL_TOTAL_DURATION=500 CHIPROOT=/n/auspex/s10/chip/euterpe
/n/auspex/s10/chip/euterpe/tools/bin/pifpack hc0-pass1.pim.pif -obstructionPdl
/n/auspex/s10/chip/euterpe/gards/sofa/sofa.pdl \
-obstructionCdl
/n/auspex/s10/chip/euterpe/gards/sofa/sofa.cdl \
-libraryPdl gards/hc0-pass1macros.pdl -ecl -tech mobi \
-trueSqueeze 40 -distance 6 -packBothEdges
/n/auspex/s10/chip/euterpe/tools/bin/pifpack: Preparing input files...
/n/auspex/s10/chip/euterpe/gards/sofa/sofa.cdl...
/n/auspex/s10/chip/euterpe/tools/bin/pifpack: Reading
/n/auspex/s10/chip/euterpe/gards/sofa/sofa.cdl...
/n/auspex/s10/chip/euterpe/tools/bin/pifpack: Reading
/n/auspex/s10/chip/euterpe/gards/sofa/sofa.pdl...
/n/auspex/s10/chip/euterpe/tools/bin/pifpack: Packing right edge...
/n/auspex/s10/chip/euterpe/tools/bin/pim2pif.ex: Final width 191 ECL atoms, squeezed out
24 ECL atoms ...which may include up to 0 ECL atoms of obstructions
/n/auspex/s10/chip/euterpe/tools/bin/pim2pif.ex: 52 rows (52 non-empty) ...spanning 27
columns (28 maximum cells/row) ...for a total of 1088 cells were written to `hc0-
pass1.pim.pif.packed'.
/n/auspex/s10/chip/euterpe/tools/bin/pim2pif.ex: (1914, 491) to (2296,
653) [191 by 54 ECL atoms]
/n/auspex/s10/chip/euterpe/tools/bin/pim2pif.ex: 8946 ECL atoms placed in
10314 [-382 obstructions] atom area [90.07% dense] #pim2pif.ex Version 0.2.14 Tue Sep 13
17:03:51 PDT 1994
/n/auspex/s10/chip/euterpe/tools/bin/pifpack: Packing left edge...
/n/auspex/s10/chip/euterpe/tools/bin/pim2pif.ex: Final width 191 ECL atoms, squeezed out 0
ECL atoms ...which may include up to 0 ECL atoms of obstructions
/n/auspex/s10/chip/euterpe/tools/bin/pim2pif.ex: 52 rows (52 non-empty) ...spanning 27
columns (28 maximum cells/row) ...for a total of 1088 cells were written to `hc0-
pass1.pim.pif.packed'.
/n/auspex/s10/chip/euterpe/tools/bin/pim2pif.ex: (1914, 491) to (2296,
653) [191 by 54 ECL atoms]
/n/auspex/s10/chip/euterpe/tools/bin/pim2pif.ex: 8946 ECL atoms placed in
10314 [-382 obstructions] atom area [90.07% dense] #pim2pif.ex Version 0.2.14 Tue Sep 13
17:03:51 PDT 1994 HOME=/n/auspex/s10/chip/euterpe/tools
LM_LICENSE_FILE=/n/auspex/s10/chip/euterpe/tools/sl/license/license.dat
DISPLAY=clio:0.0 SL_TOTAL_DURATION=500 CHIPROOT=/n/auspex/s10/chip/euterpe

```

```

/n/auspex/s10/chip/euterpe/tools/bin/pif2pim hc0-pass1.pim.pif.packed -xrf gards/hc0-
pass1.xrf -dff gards/hc0-pass1.dff \
-obstructionPd1 /n/auspex/s10/chip/euterpe/gards/sofa/sofa.pd1 \
-obstructionCd1 /n/auspex/s10/chip/euterpe/gards/sofa/sofa.cd1 \
-libraryPd1 gards/hc0-pass1macros.pd1 -ecl -tech mobi -sdl \
-collapseRows -noSpacers -noAlign -noOffset
/n/auspex/s10/chip/euterpe/tools/bin/pif2pim: Preparing input files...
/n/auspex/s10/chip/euterpe/tools/bin/pif2pim: Reading gards/hc0-pass1.dff...
/n/auspex/s10/chip/euterpe/tools/bin/pif2pim: Reading
/n/auspex/s10/chip/euterpe/gards/sofa/sofa.pd1...
/n/auspex/s10/chip/euterpe/tools/bin/pif2pim: Fetching bounding box from
/n/auspex/s10/chip/euterpe/gards/sofa/sofa.cd1...
/n/auspex/s10/chip/euterpe/tools/bin/pif2pim: Reading
/n/auspex/s10/chip/euterpe/gards/sofa/sofa.cd1...
//n/auspex/s10/chip/euterpe/tools/bin/pim2pif.ex: 160 rows 29 columns written to `hc0-
pass1.pim.pif.packed.pim'
#pim2pif.ex Version 0.2.14 Tue Sep 13 17:03:51 PDT 1994 mv hc0-pass1.pim.pif.packed
wards/hc0-pass1.pif
**** GPLACE hc0-pass1
Tue Sep 20 09:18:17 PDT 1994
sed -e 's!DESIGN_NAME!hc0-pass1!' -e 's!EDIF_FILE!hc0-pass1.sdl!' -e 's!
CHIPROOT!/n/auspex/s10/chip/euterpe!' -e 's!TECH_GPLACE!gplace.mobi234!' -e 's!TECH_REDIT!
redit.mobi234!' < /n/auspex/s10/chip/euterpe/proteus/misc/gards.vrf > gards/hc0-pass1.vrf
rm -f gards/gplace.nic cd gards; if HOME=/n/auspex/s10/chip/euterpe/tools
LM_LICENSE_FILE=/n/auspex/s10/chip/euterpe/tools/sl/license/license.dat
DISPLAY=clio:0.0 SL_TOTAL_DURATION=500 CHIPROOT=/n/auspex/s10/chip/euterpe
/n/auspex/s10/chip/euterpe/tools/bin/gastatus -p -s hc0-pass1; then \
/usr/5bin/echo 'deletgroup use; ok' > gplace.nic; fi /usr/5bin/echo 'readpif hc0-
pass1.pif; ok\nwritenof hc0-pass1.nof; use; ok\nexitsave\nexitnosave' >> gards/gplace.nic
(echo "cd `abspath`/wards; \
HOME=/n/auspex/s10/chip/euterpe/tools
LM_LICENSE_FILE=/n/auspex/s10/chip/euterpe/tools/sl/license/license.dat
DISPLAY=clio:0.0 SL_TOTAL_DURATION=500 CHIPROOT=/n/auspex/s10/chip/euterpe
/n/auspex/s10/chip/euterpe/tools/sl/bin/invoke gplace hc0-pass1 -listing hc0-
pass1.gplace.lis -cmdin gplace.nic -colorin gplace.mobi234 -inbat 1"
| \
/usr/local/bin/rexec ghidra sh &&
HOME=/n/auspex/s10/chip/euterpe/tools
LM_LICENSE_FILE=/n/auspex/s10/chip/euterpe/tools/sl/license/license.dat
DISPLAY=clio:0.0 SL_TOTAL_DURATION=500 CHIPROOT=/n/auspex/s10/chip/euterpe
/n/auspex/s10/chip/euterpe/tools/bin/gastatus -sp gards/hc0-pass1) || (mv gards/hc0-
pass1.nof gards/hc0-pass1.nof.ERROR; rm -f hc0-pass1.nof; false)

Requires a minimum license of xgplacel_3 or gardsl_3 .
Applicable licenses available at your installation :
gardsconfig_3
Checked out one user token of a gardsconfig_3 license.

GARDES GPLACE 7.119 -- General Placer
Copyright (c) 1994 SILVAR-LISCO. All rights reserved.
Design: hc0-pass1 Started at: 94/09/20 09:18:21

```

GPLACE Version 7.1.19 of November 22, 1993

```

No component hierarchy found; select by hierarchy disabled.
Loading components...
Loading nets...
Loading logical types...
Processing physical types...
Loading cell_types...
Creating net-comp xref table...

```

```

Terminated at      : 94/09/20 09:22:06
Elapsed CPU time   : 0 Hrs   3 Mins 23 Secs
Elapsed wall clock time : 0 Hrs   3 Mins 45 Secs

```

```
rm -f gards/gplace.nic
/n/auspex/s10/chip/euterpe/tools/bin/gasavepins gards/hc0-pass1.dff
Updating: gards/hc0-pass1.dff
gmake[2]: *** [gars/hc0-pass1.nof] Segmentation fault (core dumped)
gmake[2]: *** Deleting file `gars/hc0-pass1.nof'
gmake[2]: *** [gars/hc0-pass1.nof] Deleting file `gars/hc0-pass1.gplace.lis'
gmake[2]: Leaving directory
~/N/auspex/root/s10/chip/euterpe/verilog/bsrc/hc'
gmake[1]: *** [hc0.short.nets] Error 1
gmake[1]: Leaving directory
~/N/auspex/root/s10/chip/euterpe/verilog/bsrc/hc'
gmake: *** [hc0gars] Error 1
[finished at Tue Sep 20 09:22:11 PDT 1994 -- exit status 0]
```

From: Graham Y. Mostyn [graham@thalia]
Sent: Tuesday, September 20, 1994 1:16 PM
To: 'hestia@thalia'; 'tbe@microunity.com'
Cc: 'pmayer@thalia'
Subject: Re: minutes/actions from 9/19 pcb meeting

We also briefly discussed the issue of 2 prong vs 3 prong convenience outlet. Our internally generated multimedia spec 3/31/94 did state 3 prong. The situation is that:

(1) The Toltec spec 3/16/94 calls for a 2 prong outlet.

(2) Per Wayne, UL does not require a 3 prong outlet even though the line cord has a 3 prong plug. (However, if Hestia is sold with another device requiring a 3-connection supply and ground, a warning statement must be included stating that the 2 prong convenience outlet may not be used to power the other device.)

(3) We have not yet located or designed in a 3 prong, and a design change would cause schedule impact.

In a separate discussion this morning, Jack Holloway agreed to our position at the meeting, which was to continue on the current path of designing a 2 prong convenience outlet for initial Hestia units. However, he stated that the trend was to 3 prong, and that we should plan a later design conversion to 3 prong.

Tom, would the design change to 3 prong later be significantly more painful over changing now? Only in that event should we reconsider our decision.

Graham.

> From tbe@MicroUnity.com Mon Sep 19 19:44:16 1994
> Date: Mon, 19 Sep 94 19:44:08 PDT
> X-Sender: tbe@gaea.microunity.com
> Mime-Version: 1.0
> Content-Type: > text/plain> ; > charset="us-ascii">
> To: hestia
> From: tbe@MicroUnity.com
> Subject: minutes/actions from 9/19 pcb meeting
> Cc: pmayer
> Content-Length: 1738
>
> Following are minutes and action items from today's pcb meeting:
>
> 1) Main pcb split: issue of moving the dc-dc to the ac-dc pcb to
eliminate
> risk of Hipot failures (immediate or latent) in low voltage components.
> Wayne discussed concern with manufacturing defects causing failures
during
> production startup. Decision taken not to change current design for
first
> 50 (nondeliverable) units, so as not to impact schedule or product cost.
>
> action: tbe to revive investigation of high-current power bussing from
> early days of Hestia for contingency of changing design to isolate
> high voltage stuff in the future. This should be complete with a
> preliminary design by the time the first protos are built.
>
> action: Wayne wants to analyze the implications of dc-dc on main pcb
> for Hipot test and possibly come up with additional tests to mitigate
> risk
of
> damage.
>
>
> 2) The main pcb will require break-away edge tabs for manufacturing

fixture
> requirements (TAB OLB, solder reflow machines, etc).
>
> action: tbe to incorporate into next revision of criteria drawing.
>
>
> 3) Wayne asked for vias on HC bus between Calliope and Euterpe.
>
> action: tbe to get minimum via spacing to wayne for evaluation wrt ICT.
>
> action: tbe to verify with Hadco manufacturability of via array.
>
> action: tbe to revise spacer cutout to maximize area for via fanout
>
>
> 4) Jay mentioned that the smart card connector is not shown on the
mainpcb
> criteria.
>
> action: tbe to incorporate into next revision. Patty can place where
> convenient for time being.
>
> If I missed anything, please jump in!
>
> -Tom
>
>
>
> Tom Eich tbe@microunity.com
> MicroUnity Systems Engineering, Inc.
> 255 Caspian Dr. Sunnyvale, CA 94089
> (408)734-8100, (408)734-8136 fax
>
>
>

From: lisa
Sent: Tuesday, September 20, 1994 1:51 PM
To: 'Guillermo A. Loyola'
Cc: 'jimura'
Subject: Re: gnu-tools/ld configure.in

Your list was correct except for a couple of missing aliases (terpbo, terp).
BTW, for fun you can do "...gnu-tools/config.sub xxxx" and it will spit back the canonical form for the alias "xxxx".

Arch	Endian	OS	Canonical Aliases	bfd
Big Old	BE	STB	terpbo-muse-stb	
elf64-bigold	terp		terpbo-stb, terpbo-muse, terpbo	
Big Old	BE	OSF	terpbo-muse-osf	
elf64-bigold	terp		terpbo-osf	
Terp	LE	STB	terp-muse-stb	
elf64-little	terp		terp-stb, terp-muse, terp	
Terp	LE	OSF	terp-muse-osf	
elf64-little	terp		terp-osf	

There is no way to configure the old architecture with little-endian data:

Big Old LE STB --N/A--
Big Old LE OSF --N/A--

Since there was no plan to use a big-data/current-arch environment, I didn't fill this out, but the following are intended:

Terp	BE	STB	terpbig-muse-stb
elf64-big	terp		terpbig-stb, terpbig-muse, terpbig
Terp	BE	OSF	terpbig-muse-osf
elf64-big	terp		terpbig-osf

I'm sure these configurations won't work without some help. There also isn't much precedence for this kind of variation, and I'm fairly sure these names are not good choices: usually specifying the architecture and either the os or the machine determines the endianness--e.g.

mips-alpha is little-endian, mips-irix* is big-endian. But all that is really just a matter of what configurations we want to provide, and what we want to call them; the underlying mechanism is all ready (i.e. architecture and data-endianness are separate in the eyes of bfd, simulator, etc.).

FYI, tgcc will not work properly wrt register-pairs in this combo; no fault of the configuration, but with assumptions in gcc. I know what needs to be done; I don't think it is a whole lot.

Not being able to configure that environment, though, is not the same as not being able to use it--you can get at the big-endian-data-running- on-a-current-architecture-terp environment by doing:

```
tgcc -mbig # Note register-pair problem, however
tas -big
tld -format elf64-bigterp
```

The simulator, gdb, objdump, etc. will recognize such executables.

I was actually intending to fix gcc and then see if I could build a few (working ;-) user-level things this way...

lisa

From: lisa
Sent: Tuesday, September 20, 1994 2:17 PM
To: 'software-checkins-dist'
Subject: gnu-tools/sim/terp sim.h terp.h

Update of /p/cvsroot/gnu-tools/sim/terp
In directory calliope:/N/hyperion/root/s1/lisa/gnu-tools/sim/terp

Modified Files:
 sim.h terp.h
Log Message:

Moved definition of TERP_ENDIAN and TERP_ENDIAN_VARIES from sim.h to terp.h.

From: lisa
Sent: Tuesday, September 20, 1994 2:19 PM
To: 'software-checkins-dist'
Subject: gnu-tools/sim/terp memory.h

Update of /p/cvsroot/gnu-tools/sim/terp
In directory calliope:/N/hyperion/root/s1/lisa/gnu-tools/sim/terp

Modified Files:

memory.h

Log Message:

Move_data_aligned needs to swap hexlet halves when TERP_ENDIAN != HOST_ENDIAN.

From: lisa
Sent: Tuesday, September 20, 1994 2:20 PM
To: 'software-checkins-dist'
Subject: gnu-tools/sim/terp execloop.c

Update of /p/cvsroot/gnu-tools/sim/terp
In directory calliope:/N/hyperion/root/sl/lisa/gnu-tools/sim/terp

Modified Files:
 execloop.c

Log Message:

Define loadLE, storeLE, loadBE, storeBE based on HOST_ENDIAN, rather than assuming all
hosts are big-endian. Just planning ahead...

From: Buffalo Chip [chip@staypuft]
Sent: Tuesday, September 20, 1994 2:50 PM
To: 'geert@staypuft'
Subject: output of euterpe/verilog/bsrc/hc.checkoutrc

Tue Sep 20 12:35:49 PDT 1994 (geert Tue, 20 Sep 1994 12:35:26 -0700)
euterpe/verilog/bsrc/hc
[Release BOM (V38.0) in euterpe/verilog/bsrc/hc (Tue Sep 20 12:35:50 PDT 1994)]

Dir euterpe/verilog/bsrc/hc BOM 38.0

35.1 .checkoutrc
1.19 Makefile
34.1 genpim0.pl
32.4 genpim1.pl
(32.3)
12.5 gentst.pl
1.26 hc.V
3.6 hc.h
8.5 hc.ut
17.1 hc_buf_8.V
6.1 hc_cmp6.V
27.5 hc_control.pim
8.7 hc_device.V
3.15 hc_driver.V
4.1 hc_error.Veqn
12.1 hc_fifo8.V
12.1 hc_fifo8ctrl.Veqn
3.10 hc_ostate.pla
3.2 hc_parse.Veqn
3.6 hc_prbctrl.pla
3.1 hc_rxcrc.Veqn
3.3 hc_sdecode.Veqn
3.7 hc_sid.Veqn
3.2 hc_tagmatch.V
3.2 hc_txcrc.Veqn
13.1 hcinstantiate.h
27.2 pimlib.pl
17.3 power.tab.local

===> running euterpe/verilog/bsrc/hc/.checkoutrc (Tue Sep 20 12:35:58 PDT
1994) <===

```
#
# turn off pgroute
#
[ -f nopgroute ] || touch nopgroute
#
# use padtiles
#
[ -f usepadtiles ] || touch usepadtiles
#
# use pifpack
#
[ -f usepifpack ] || touch usepifpack
#
# insert an instance of the clock tree
#
[ -f addclock ] || touch addclock
#
# Disable old dcell placement obstruction # [ -f gards/noobs ] || touch gards/noobs # #
Now do it . . .
#
gmake GARDS_DISPLAY=clio:0.0 hc0-iter
gmake[1]: Entering directory
~/N/auspex/root/s10/chip/euterpe/verilog/bsrc/hc'
```

```
#
# Get an initial sdl file. A manhattan approximation will be used # gmake
GARDS_DISPLAY=clio:0.0 CYCLETIME=895 gards/hc0-pass2.sdl
gmake[2]: Entering directory
~/N/auspex/root/s10/chip/euterpe/verilog/bsrc/hc'
CHIPROOT=/n/auspex/s10/chip/euterpe
/n/auspex/s10/chip/euterpe/tools/bin/topt -p
/n/auspex/s10/chip/euterpe/proteus/misc/power.tab -p power.tab.local -h
/n/auspex/s10/chip/euterpe/proteus/leafgen/dclload/dclload.lib -h
/n/auspex/s10/chip/euterpe/proteus/exlax/dclload/dclload.lib -h
/n/auspex/s10/chip/euterpe/proteus/custom/dclload/dclload.lib -g
/n/auspex/s10/chip/euterpe/proteus/leafgen/toptList -g
/n/auspex/s10/chip/euterpe/proteus/exlax/toptList -g
/n/auspex/s10/chip/euterpe/proteus/custom/toptList \
-A /n/auspex/s10/chip/euterpe/proteus/leafgen/caps/cap.lib -A
/n/auspex/s10/chip/euterpe/proteus/exlax/caps/cap.lib -A
/n/auspex/s10/chip/euterpe/proteus/custom/caps/cap.lib \
-H /n/auspex/s10/chip/euterpe/proteus/leafgen/time/tim.lib -H
/n/auspex/s10/chip/euterpe/proteus/custom/time/tim.lib -d
/n/auspex/s10/chip/euterpe/proteus/exlax/time/tim.lib \
-l 895 \
-e hc0.edif \
-k hc0-pass1.strength -B gards/hc0-pass1.sdl -s gards/hc0-pass1.stat -O gards/hc0-
pass1.topt.log \
-z 2 -M mobimos -R -t 50 -b 10 -a 24 -0 -F
```

Running topt (Power Optimizer) compiled on Tue Sep 20 17:41:45 GMT 1994

```
Processing a: Mobimos, Flop/Latch design
Consuming edif file hc0.edif
Found edif structure: hc0_46_edif
Flattening edif;
HC already flat.
found 1120 instances; found 2846 nets in hc0_46_edif
Consuming power table information file
/n/auspex/s10/chip/euterpe/proteus/misc/power.tab
Consuming power table information file power.tab.local
Reading Stats file
/n/auspex/s10/chip/euterpe/proteus/leafgen/stats.ec1
Reading Stats file
/n/auspex/s10/chip/euterpe/proteus/leafgen/stats.cmos
Reading Stats file /n/auspex/s10/chip/euterpe/proteus/exlax/stats.ea
Reading Stats file
/n/auspex/s10/chip/euterpe/proteus/custom/stats.ec1
Reading Legal Cell List file
/n/auspex/s10/chip/euterpe/proteus/leafgen/toptList
Reading Legal Cell List file
/n/auspex/s10/chip/euterpe/proteus/exlax/toptList
ReadLegalCellFile: Warning! No atoms info for ealnf36s9x4a
Reading Legal Cell List file
/n/auspex/s10/chip/euterpe/proteus/custom/toptList
Performing Edif Transformations...
Reading DC Loads file
/n/auspex/s10/chip/euterpe/proteus/leafgen/dclload/dclload.lib
Reading DC Loads file
/n/auspex/s10/chip/euterpe/proteus/exlax/dclload/dclload.lib
Reading DC Loads file
/n/auspex/s10/chip/euterpe/proteus/custom/dclload/dclload.lib
Reading intrinsic delays from
/n/auspex/s10/chip/euterpe/proteus/exlax/time/tim.lib

Reading pin cap values from
/n/auspex/s10/chip/euterpe/proteus/leafgen/caps/cap.lib
Reading pin cap values from
/n/auspex/s10/chip/euterpe/proteus/exlax/caps/cap.lib
Reading pin cap values from
/n/auspex/s10/chip/euterpe/proteus/custom/caps/cap.lib
Status information in gards/hc0-pass1.stat Warning! Cell cgclockbias not on legal
```



```
Any gate in it's path is not AC power optimized
No swing calculations will be performed
Pruning flattened network of unused instances... 31 pruned in 2
passes.
```

Found 19 Warnings! Please check stat file!

```
Warning! Cell cache at line 4 is not in legal cell list Warning! Cell cahalf at line 10
is not in legal cell list Warning! Cell cr at line 13 is not in legal cell list Warning!
Cell cttag at line 20 is not in legal cell list Warning! Cell gtlb at line 23 is not in
legal cell list Warning! Cell scgcbfr0 at line 52 is not in legal cell list Warning!
Cell scsof3v3 at line 188 is not in legal cell list
```

Connected 0 inputs to net vref 0ph...

[illegible]

No XFER_BM<3> pin capacitance data for cgclockbias Warning! No XFER_BM<2> pin capacitance data for cgclockbias Warning! No XFER_BM<1> pin capacitance data for cgclockbias Warning! No XFER_BM<0> pin capacitance data for cgclockbias Warning! No PHI_A2P pin capacitance data for scsynchl1 Warning! No PHI_B2P pin capacitance data for scsynchl1 Warning! No D0_AD0PF pin capacitance data for scsynchl1 Warning! No D0_AD0PF pin capacitance data for scsynchl1

Ignoring these nets:

PHI_B2P PHI_A2P vref_0ph

Optimizing power...

Iteration: 1

Path power optimizer

IntrinsicWarning: Warning! No clk_to_q flipflop fanin 1 delay for flipflop scsynchl1

NOTE: Cell scsynchl1 using 'intrinsic delay + .7RC' calculations.

IntrinsicWarning: Warning! No setup gate fanin 1 delay for flipflop scsynchl1 for input pin D0_AD0PF

ERROR! 3 paths exceeded cycle time. Check status file.

DC Load Calculations

Unpowered Instance check: 2 found.

Iteration: 2

Path power optimizer

IntrinsicWarning: Warning! No clk_to_q gate fanin 1 delay for gate xbcmos2ecldf2s for input pin CIN ABM

ERROR! 3 paths exceeded cycle time. Check status file.

DC Load Calculations

Unpowered Instance check: 1 found.

Iteration: 3

Path power optimizer

ERROR! 3 paths exceeded cycle time. Check status file.

DC Load Calculations

Unpowered Instance check: 1 found.

Squeezing out extra time in paths.

Iteration: 4

Path power optimizer

ERROR! 3 paths exceeded cycle time. Check status file.

DC Load Calculations

Unpowered Instance check: 1 found.

Iteration: 5

Path power optimizer

ERROR! 3 paths exceeded cycle time. Check status file.

DC Load Calculations

Unpowered Instance check: 1 found.

Iteration: 6

Path power optimizer

ERROR! 3 paths exceeded cycle time. Check status file.

DC Load Calculations

Unpowered Instance check: 1 found.

Savings by squeezing out extra time = (5771 - 5789) = -0.31% Change from original input power = (5789 - 152) = 97.37%

Warning! 1 unpowered or untouched instances.

Warning! There are missing DC load values.

NOTE: 692 unpowered nets.

NOTE: 55 nets with delays less than 50.00ps

NOTE: Power levels changed for 1060 instances.

Atoms:	count	atom	bjt	isrc	pld	clock
BJT Totals:	1089	8796	19267	12189	11520	5888

Generating instance drive strength file hc0-pass1.strength

```

Disgorging sdl file gards/hc0-pass1.sdl
Writing sdl structure: hc0_46_edif
Memory usage: 26.395MB
Exit code would be 2 (Failed Max Timing), but is forced to 0
CHIPROOT=/n/auspex/s10/chip/euterpe
/n/auspex/s10/chip/euterpe/tools/bin/pdcat -p
/n/auspex/s10/chip/euterpe/clockbias:/n/auspex/s10/chip/euterpe/gards/subb
locks:/n/auspex/s10/chip/euterpe/gards/dcell:/n/auspex/s10/chip/euterpe/pr
oteus/gards/leaf:/n/auspex/s10/chip/euterpe/proteus/gards/sofa:/n/auspex/s
10/chip/euterpe/proteus/gards/dcell `grep -v '^#' < hc0-pass1.strength | awk '{print
$4;}' | sort | uniq | awk '{printf ("%s.pdl ", $1)}'` > gards/hc0-pass1macros.temp mv
gards/hc0-pass1macros.temp gards/hc0-pass1macros.pdl
**** SLNET hc0-pass1
Tue Sep 20 12:40:01 PDT 1994
sed -e 's!DESIGN_NAME!hc0-pass1!' -e 's!EDIF_FILE!hc0-pass1.sdl!' -e 's!
CHIPROOT!/n/auspex/s10/chip/euterpe!' -e 's!TECH_GPLACE!gplace.mobi234!' -e 's!TECH_REDIT!
redit.mobi234!' < /n/auspex/s10/chip/euterpe/proteus/misc/gards.vrf > gards/hc0-pass1.vrf
echo `cd `abspath`/gards; \
echo translate_all | HOME=/n/auspex/s10/chip/euterpe/tools
LM_LICENSE_FILE=/n/auspex/s10/chip/euterpe/tools/sl/license/license.dat
DISPLAY=clio:0.0 SL_TOTAL_DURATION=500 CHIPROOT=/n/auspex/s10/chip/euterpe
/n/auspex/s10/chip/euterpe/tools/sl/net/dir/slnet hc0-pass1" | /usr/local/bin/rexec
staypuft sh
** SLNET 1.037 ** SL NET V1.000 -- Netlist Manipulator Copyright (c) 1993,1994 SILVAR-
LISCO. All rights reserved.
Design: hc0-pass1 Started at: 94/09/20 12:40:05

```

Loading file "hc0-pass1.sdl".

```

[XBC01DF24S]
[XBC01DF6S]
[XBC01DF12S]
[XBCMOS2ECLDF2S]
[XBBUFD16S]
[XBFFBDH6S]
[XBFFBDF32S]
[XBFFDF24S]
[XBFFBDH12S]
[XBFFDH24S]
[XBFFDH3S]
[XBFFDH16S]
[XBFFDH2S]
[XBFFDF2S]
[XBFFDF4S]
[XBFFDF6S]
[XBFFDF8S]
[XBFFDF32S]
[XBFFDF12S]
[XBFFDF16S]
[XBOR3DF6S]
[XBOR3DF8S]
[XBOR3DF4S]
[XBOR3DF2S]
[XBOR11DF4S]
[XBORFF5DF24S]
[XBORFF5DH3S]
[XBORFF5DH12S]
[XBORFF5DF32S]
[XBORFF5DF4S]
[XBORFF5DF8S]
[XBORFF2DH8S]
[XBORFF2DF2S]
[XBORFF2DF24S]
[XBORFFB2DH4S]
[XBORFF2DH4S]
[XBORFF2DH16S]
[XBORFFB2DH16S]

```

[XBORFFB2DH12S]
[XBORFF2DH24S]
[XBORFF2DF12S]
[XBORFF2DF8S]
[XBORFF2DF4S]
[XBORFF2DF6S]
[XBMUXFF2DF12S]
[XBMUXFF2DF4S]
[XBMUXFF2DH12S]
[XBMUXFF2DF8S]
[XBMUXFF2DH2S]
[XBMUXFF2DH3S]
[XBMUXFFB2DH3S]
[XBOR4DF6S]
[XBOR4DF4S]
[XBOR4DF16S]
[XBOR4DF8S]
[XBOR4DF2S]
[XBOR5DF12S]
[XBOR5DF16S]
[XBOR5DF4S]
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[XBOR5DF8S]
[XBOR6DF16S]
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[XBOR6DF4S]
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[XBOR7DF4S]
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[XBOR8DF12S]
[XBOR8DF2S]
[XBOR9DF8S]
[XBOR9DF4S]
[XBOR10DF4S]
[XBOR2DF2S]
[XBOR2DF4S]
[XBORFFB3DH4S]
[XBORFF3DF12S]
[XBORFF3DF24S]
[XBORFF3DF32S]
[XBORFF3DH2S]
[XBORFF3DF6S]
[XBORFF3DF16S]
[XBORFF3DF8S]
[XBORFF3DF4S]
[XBORFF3DH8S]
[XBORFF7DF4S]
[XBORFF7DF12S]
[XBORFFB7DF12S]
[XBORFF7DF2S]
[XBORFF4DH3S]
[XBORFF4DH6S]
[XBORFF4DF16S]
[XBORFF4DH2S]
[XBORFFB4DH12S]
[XBORFF4DF24S]
[XBORFF4DF6S]
[XBORFF9DH3S]
[XBORFF17DH3S]
[XBORFF6DH4S]
[XBORFF6DF6S]
[XBORFF6DF4S]

[XBORFF13DF24S]
[XBORFF11DF24S]
[XBORFF8DF24S]
[XBORFF8DF32S]
[XBMUXFF8DF4S]
[XBMUXFF8DH2S]
[XBXOR2DF4S]
[XBMUXFF4DF4S]
[XBMUXFF4DH2S]
[XBMUXFF6DH24S]
[XBMUXFF9DF6S]
[XBMUXFF3DH24S]
[XBBUFDH2S]
[XBBUFDH16S]
[SCSYNCHLL]
[CGCLOCKBIAS]
[HC]

** Warning: No nets connected to component CGCLOCKBIAS.

Translating...

[XBC01DF24S]
[XBC01DF6S]
[XBC01DF12S]
[XBCMOS2ECLDF2S]
[XBBUFDH16S]
[XBFFBDH6S]
[XBFFBDF32S]
[XBFFDF24S]
[XBFFBDH12S]
[XBFFDH24S]
[XBFFDH3S]
[XBFFDH16S]
[XBFFDH2S]
[XBFFDF2S]
[XBFFDF4S]
[XBFFDF6S]
[XBFFDF8S]
[XBFFDF32S]
[XBFFDF12S]
[XBFFDF16S]
[XBOR3DF6S]
[XBOR3DF8S]
[XBOR3DF4S]
[XBOR3DF2S]
[XBOR11DF4S]
[XBORFF5DF24S]
[XBORFF5DH3S]
[XBORFF5DH12S]
[XBORFF5DF32S]
[XBORFF5DF4S]
[XBORFF5DF8S]
[XBORFF2DH8S]
[XBORFF2DF2S]
[XBORFF2DF24S]
[XBORFFB2DH4S]
[XBORFF2DH4S]
[XBORFF2DH16S]
[XBORFFB2DH16S]
[XBORFFB2DH12S]
[XBORFF2DH24S]
[XBORFF2DF12S]
[XBORFF2DF8S]
[XBORFF2DF4S]
[XBORFF2DF6S]
[XBMUXFF2DF12S]
[XBMUXFF2DF4S]
[XBMUXFF2DH12S]
[XBMUXFF2DF8S]
[XBMUXFF2DH2S]

[XBMUXFF2DH3S]
[XBMUXFFB2DH3S]
[XBOR4DF6S]
[XBOR4DF4S]
[XBOR4DF16S]
[XBOR4DF8S]
[XBOR4DF2S]
[XBOR5DF12S]
[XBOR5DF16S]
[XBOR5DF4S]
[XBOR5DF2S]
[XBOR5DF6S]
[XBOR5DF8S]
[XBOR6DF16S]
[XBOR6DF6S]
[XBOR6DF12S]
[XBOR6DF2S]
[XBOR6DF4S]
[XBOR7DF2S]
[XBOR7DF16S]
[XBOR7DF4S]
[XBOR7DF6S]
[XBOR8DF4S]
[XBOR8DF8S]
[XBOR8DF12S]
[XBOR8DF2S]
[XBOR9DF8S]
[XBOR9DF4S]
[XBOR10DF4S]
[XBOR2DF2S]
[XBOR2DF4S]
[XBORFFB3DH4S]
[XBORFF3DF12S]
[XBORFF3DF24S]
[XBORFF3DF32S]
[XBORFF3DH2S]
[XBORFF3DF6S]
[XBORFF3DF16S]
[XBORFF3DF8S]
[XBORFF3DF4S]
[XBORFF3DH8S]
[XBORFF7DF4S]
[XBORFF7DF12S]
[XBORFFB7DF12S]
[XBORFF7DF2S]
[XBORFF4DH3S]
[XBORFF4DH6S]
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[XBORFFB4DH12S]
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[XBORFF6DH4S]
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[XBORFF6DF4S]
[XBORFF13DF24S]
[XBORFF11DF24S]
[XBORFF8DF24S]
[XBORFF8DF32S]
[XBMUXFF8DF4S]
[XBMUXFF8DH2S]
[XBXOR2DF4S]
[XBMUXFF4DF4S]
[XBMUXFF4DH2S]
[XBMUXFF6DH24S]
[XBMUXFF9DF6S]

[XBMUXFF3DH24S]
 [XBBUFD2S]
 [XBBUFDH16S]
 [SCSYNCHLL]
 [CGCLOCKBIAS]
 [HC]

Netlist Info :

 Number of logic types : 122
 Number of nets : 2302
 Number of components : 1089
 Number of component pins : 10875
 Number of pins/comp : 9.986226
 Number of nets/comp : 2.113866

Size estimation :

size	TYPE	# inst	size/inst	total
-----+-----+-----+-----+				
	XBMUXFF2DF4S	4	1	4
	XBORFFB3DH4S	1	1	1
	XBORFF4DF16S	2	1	2
	XBORFF8DF24S	2	1	2
	XBBUFD2S	16	1	16
	XBFFDF24S	4	1	4
	XBFFDH16S	4	1	4
	XBORFF4DH3S	3	1	3
	XBORFF5DF32S	1	1	1
	XBFFDH2S	24	1	24
	XBMUXFF6DH24S	9	1	9
	XBOR4DF6S	2	1	2
	XBOR11DF4S	5	1	5
	XBOR8DF12S	1	1	1
	XBOR2DF4S	21	1	21
	XBORFF5DF8S	1	1	1
	XBORFF2DH16S	1	1	1
	XBC01DF12S	1	1	1
	XBORFF5DH12S	1	1	1
	CGCLOCKBIAS	1	1	1
	XBMUXFF4DF4S	8	1	8
	XBMUXFF2DH3S	37	1	37

XBFFDF32S	7	1	7
XBORFF2DF2S	2	1	2
XBORFF6DF4S	1	1	1
XBMUXFF8DH2S	7	1	7
XBOR6DF6S	2	1	2
XBOR8DF8S	1	1	1
XBOR4DF4S	3	1	3
XBORFF2DF12S	10	1	10
XBOR2DF2S	59	1	59
XBOR5DF16S	2	1	2
XBORFF3DF24S	1	1	1
XBORFF3DF6S	3	1	3
XBORFF17DH3S	1	1	1
XBMUXFF2DH12S	6	1	6
XBOR4DF2S	46	1	46
XBOR6DF4S	5	1	5
XBORFFB2DH12S	2	1	2
XBC01DF24S	1	1	1
XBORFF4DH6S	8	1	8
XBMUXFF8DF4S	8	1	8
XBOR7DF16S	1	1	1
XBORFF5DF24S	2	1	2
XBORFF3DH8S	1	1	1
XBFFDF2S	2	1	2
XBMUXFF3DH24S	32	1	32
XBORFF4DH2S	7	1	7
XBORFF2DF8S	1	1	1
XBOR3DF8S	1	1	1
XBOR5DF12S	2	1	2
XBOR8DF4S	2	1	2
XBOR6DF2S	4	1	4
XBORFFB4DH12S	1	1	1
XBORFFB2DH4S	4	1	4
XBORFF3DF16S	3	1	3

XBMUXFFB2DH3S	6	1	6
XBORFF3DF4S	3	1	3
XBFFDF4S	3	1	3
XBOR10DF4S	3	1	3
XBOR8DF2S	1	1	1
XBOR3DF6S	4	1	4
XBOR5DF8S	2	1	2
XBBUPDF16S	3	1	3
XBORFF2DH4S	6	1	6
XBMUXFF2DF12S	1	1	1
XBFFBDH6S	1	1	1
XBORFF5DH3S	1	1	1
XBORFF5DF4S	2	1	2
XBFFDF6S	5	1	5
XBOR5DF6S	5	1	5
XBOR3DF4S	22	1	22
XBORFF2DF24S	1	1	1
XBORFF11DF24S	2	1	2
XBOR4DF16S	3	1	3
XBORFF2DF6S	1	1	1
XBORFF2DH24S	1	1	1
XBMUXFF9DF6S	3	1	3
XBMUXFF2DF8S	3	1	3
XBFFBDF32S	1	1	1
XBFFDH24S	1	1	1
XBFFDH3S	4	1	4
XBFFDF8S	4	1	4
XBORFF7DF4S	1	1	1
XBORFF8DF32S	1	1	1
XBOR5DF4S	2	1	2
XBOR9DF8S	1	1	1
XBORFF3DF12S	3	1	3
XBOR7DF6S	2	1	2
XBOR3DF2S	54	1	54

	SCSYNCHLL	9	1	9
	XBORFF6DH4S	1	1	1
	XBOR6DF16S	4	1	4
	XBORFF13DF24S	4	1	4
	XBORFFB7DF12S	1	1	1
	XBORFF4DF24S	3	1	3
	XBBUFDH16S	2	1	2
	XBORFF4DF6S	15	1	15
	XBORFF2DH8S	1	1	1
	XBORFF9DH3S	1	1	1
	XBFFDF12S	9	1	9
	XBORFF3DH2S	2	1	2
	XBMUXFF2DH2S	312	1	312
	XBOR7DF4S	2	1	2
	XBXOR2DF4S	48	1	48
	XBOR5DF2S	9	1	9
	XBC01DF6S	1	1	1
	XBCMOS2ECLDF2S	20	1	20
	XBORFF6DF6S	8	1	8
	XBORFFB2DH16S	1	1	1
	XBFFBDH12S	1	1	1
	XBORFF3DF32S	1	1	1
	XBORFF7DF2S	8	1	8
	XBFFDF16S	2	1	2
	XBORFF2DF4S	32	1	32
	XBMUXFF4DH2S	1	1	1
	XBOR7DF2S	3	1	3
	XBOR6DF12S	8	1	8
	XBORFF7DF12S	1	1	1
	XBORFF3DF8S	4	1	4
	XBOR9DF4S	2	1	2
	XBOR4DF8S	30	1	30
+-----+-----+-----+				
	TOTAL	1089	1	1089


```

Elapsed CPU time      : 0 Hrs   0 Mins   8 Secs
Elapsed wall clock time : 0 Hrs   0 Mins  20 Secs
Tue Sep 20 12:41:14 PDT 1994
HOME=/n/auspex/s10/chip/euterpe/tools
LM_LICENSE_FILE=/n/auspex/s10/chip/euterpe/tools/sl/license/license.dat
DISPLAY=clio:0.0 SL_TOTAL_DURATION=500 CHIPROOT=/n/auspex/s10/chip/euterpe
/n/auspex/s10/chip/euterpe/tools/bin/pim2pif hc0-pass1.pim -xrf gards/hc0-pass1.xrf -dff
gards/hc0-pass1.dff -noHole \
-obstructionPd1 /n/auspex/s10/chip/euterpe/gards/sofa/sofa.pd1 \
-obstructionCd1 /n/auspex/s10/chip/euterpe/gards/sofa/sofa.cdl \
-libraryPd1 gards/hc0-pass1macros.pd1 -ecl -tech mobi -sd1 \

/n/auspex/s10/chip/euterpe/tools/bin/pim2pif: Preparing input files...
/n/auspex/s10/chip/euterpe/tools/bin/pim2pif: Reading
/n/auspex/s10/chip/euterpe/gards/sofa/sofa.pd1...
/n/auspex/s10/chip/euterpe/tools/bin/pim2pif: Reading gards/hc0-pass1.dff...
/n/auspex/s10/chip/euterpe/tools/bin/pim2pif: Fetching bounding box from
/n/auspex/s10/chip/euterpe/gards/sofa/sofa.cdl...
/n/auspex/s10/chip/euterpe/tools/bin/pim2pif: Checking
/n/auspex/s10/chip/euterpe/gards/sofa/sofa.cdl for fixed obstructions...
/n/auspex/s10/chip/euterpe/tools/bin/pim2pif: Checking
/n/auspex/s10/chip/euterpe/gards/sofa/sofa.cdl for Ecl obstructions...
cat: write error: Broken pipe
/n/auspex/s10/chip/euterpe/tools/bin/pim2pif: Processing the hc0-pass1.pim file...
/n/auspex/s10/chip/euterpe/tools/bin/pim2pif.ex: 52 rows (52 non-empty) ...spanning 28
columns (28 maximum cells/row) ...for a total of 1088 cells were written to `hc0-
pass1.pim.pif.0'.
/n/auspex/s10/chip/euterpe/tools/bin/pim2pif.ex: (1914, 491) to (2328,
653) [207 by 54 ECL atoms]
/n/auspex/s10/chip/euterpe/tools/bin/pim2pif.ex: 8796 ECL atoms placed in
11178 [-414 obstructions] atom area [81.72% dense]
/n/auspex/s10/chip/euterpe/tools/bin/pim2pif.ex: WARNING: Potential errors, check warnings
file `hc0-pass1.pim.warn'
#pim2pif.ex Version 0.2.14 Tue Sep 13 17:03:51 PDT 1994 mv hc0-pass1.pim.warn gards
HOME=/n/auspex/s10/chip/euterpe/tools
LM_LICENSE_FILE=/n/auspex/s10/chip/euterpe/tools/sl/license/license.dat
DISPLAY=clio:0.0 SL_TOTAL_DURATION=500 CHIPROOT=/n/auspex/s10/chip/euterpe
/n/auspex/s10/chip/euterpe/tools/bin/pifpack hc0-pass1.pim.pif -obstructionPd1
/n/auspex/s10/chip/euterpe/gards/sofa/sofa.pd1 \
-obstructionCd1
/n/auspex/s10/chip/euterpe/gards/sofa/sofa.cdl \
-libraryPd1 gards/hc0-pass1macros.pd1 -ecl -tech mobi \
-trueSqueeze 40 -distance 6 -packBothEdges
/n/auspex/s10/chip/euterpe/tools/bin/pifpack: Preparing input files...
/n/auspex/s10/chip/euterpe/tools/bin/pifpack: Fetching bounding box from
/n/auspex/s10/chip/euterpe/gards/sofa/sofa.cdl...
/n/auspex/s10/chip/euterpe/tools/bin/pifpack: Reading
/n/auspex/s10/chip/euterpe/gards/sofa/sofa.cdl...
/n/auspex/s10/chip/euterpe/tools/bin/pifpack: Reading
/n/auspex/s10/chip/euterpe/gards/sofa/sofa.pd1...
/n/auspex/s10/chip/euterpe/tools/bin/pifpack: Packing right edge...
/n/auspex/s10/chip/euterpe/tools/bin/pim2pif.ex: Final width 195 ECL atoms, squeezed out
12 ECL atoms ...which may include up to 0 ECL atoms of obstructions
/n/auspex/s10/chip/euterpe/tools/bin/pim2pif.ex: 52 rows (52 non-empty) ...spanning 27
columns (28 maximum cells/row) ...for a total of 1088 cells were written to `hc0-
pass1.pim.pif.packed'.
/n/auspex/s10/chip/euterpe/tools/bin/pim2pif.ex: (1914, 491) to (2304,
653) [195 by 54 ECL atoms]
/n/auspex/s10/chip/euterpe/tools/bin/pim2pif.ex: 8796 ECL atoms placed in 10530 [-390
obstructions] atom area [86.75% dense] #pim2pif.ex Version 0.2.14 Tue Sep 13 17:03:51 PDT
1994
/n/auspex/s10/chip/euterpe/tools/bin/pifpack: Packing left edge...
/n/auspex/s10/chip/euterpe/tools/bin/pim2pif.ex: Final width 195 ECL atoms, squeezed out 0
ECL atoms ...which may include up to 0 ECL atoms of obstructions
/n/auspex/s10/chip/euterpe/tools/bin/pim2pif.ex: 52 rows (52 non-empty) ...spanning 27
columns (28 maximum cells/row) ...for a total of 1088 cells were written to `hc0-
pass1.pim.pif.packed'.
/n/auspex/s10/chip/euterpe/tools/bin/pim2pif.ex: (1914, 491) to (2304,

```

```

653) [195 by 54 ECL atoms]
/n/auspex/s10/chip/euterpe/tools/bin/pim2pif.ex: 8796 ECL atoms placed in 10530 [-390
obstructions] atom area [86.75% dense] #pim2pif.ex Version 0.2.14 Tue Sep 13 17:03:51 PDT
1994 HOME=/n/auspex/s10/chip/euterpe/tools
LM_LICENSE_FILE=/n/auspex/s10/chip/euterpe/tools/sl/license/license.dat
DISPLAY=clio:0.0 SL_TOTAL_DURATION=500 CHIPROOT=/n/auspex/s10/chip/euterpe
/n/auspex/s10/chip/euterpe/tools/bin/pif2pim hc0-pass1.pim.pif.packed -xrf gards/hc0-
pass1.xrf -dff gards/hc0-pass1.dff \
-obstructionPd1 /n/auspex/s10/chip/euterpe/gards/sofa/sofa.pd1 \
-obstructionCd1 /n/auspex/s10/chip/euterpe/gards/sofa/sofa.cdl \
-libraryPd1 gards/hc0-pass1macros.pd1 -ecl -tech mobi -sdl \
-collapseRows -noSpacers -noAlign -noOffset
/n/auspex/s10/chip/euterpe/tools/bin/pif2pim: Preparing input files...
/n/auspex/s10/chip/euterpe/tools/bin/pif2pim: Reading gards/hc0-pass1.dff...
/n/auspex/s10/chip/euterpe/tools/bin/pif2pim: Reading
/n/auspex/s10/chip/euterpe/gards/sofa/sofa.pd1...
/n/auspex/s10/chip/euterpe/tools/bin/pif2pim: Fetching bounding box from
/n/auspex/s10/chip/euterpe/gards/sofa/sofa.cdl...
/n/auspex/s10/chip/euterpe/tools/bin/pif2pim: Reading
/n/auspex/s10/chip/euterpe/gards/sofa/sofa.cdl...
//n/auspex/s10/chip/euterpe/tools/bin/pim2pif.ex: 160 rows 29 columns written to `hc0-
pass1.pim.pif.packed.pim'
#pim2pif.ex Version 0.2.14 Tue Sep 13 17:03:51 PDT 1994 mv hc0-pass1.pim.pif.packed
gards/hc0-pass1.pif
**** GPLACE hc0-pass1
Tue Sep 20 12:42:02 PDT 1994
sed -e 's!DESIGN_NAME!hc0-pass1!' -e 's!EDIF_FILE!hc0-pass1.sdl!' -e 's!
CHIPROOT!/n/auspex/s10/chip/euterpe!' -e 's!TECH_GPLACE!gplace.mobi234!' -e 's!TECH_REMIT!
redit.mobi234!' < /n/auspex/s10/chip/euterpe/proteus/misc/gards.vrf > gards/hc0-pass1.vrf
rm -f gards/gplace.nic cd gards; if HOME=/n/auspex/s10/chip/euterpe/tools
LM_LICENSE_FILE=/n/auspex/s10/chip/euterpe/tools/sl/license/license.dat
DISPLAY=clio:0.0 SL_TOTAL_DURATION=500 CHIPROOT=/n/auspex/s10/chip/euterpe
/n/auspex/s10/chip/euterpe/tools/bin/gastatus -p -s hc0-pass1; then \
/usr/5bin/echo 'deletegroup use; ok' > gplace.nic;fi /usr/5bin/echo 'readpif hc0-
pass1.pif; ok\nwritenof hc0-pass1.nof; use; ok\nexitsave\nexitnosave' >> gards/gplace.nic
(echo "cd `abspath`/gards; \
HOME=/n/auspex/s10/chip/euterpe/tools
LM_LICENSE_FILE=/n/auspex/s10/chip/euterpe/tools/sl/license/license.dat
DISPLAY=clio:0.0 SL_TOTAL_DURATION=500 CHIPROOT=/n/auspex/s10/chip/euterpe
/n/auspex/s10/chip/euterpe/tools/bin/invoke gplace hc0-pass1 -listing hc0-
pass1.gplace.lis -cmdin gplace.nic -colorin gplace.mobi234 -inbat 1"
| \
/usr/local/bin/rexec staypuft sh &&
HOME=/n/auspex/s10/chip/euterpe/tools
LM_LICENSE_FILE=/n/auspex/s10/chip/euterpe/tools/sl/license/license.dat
DISPLAY=clio:0.0 SL_TOTAL_DURATION=500 CHIPROOT=/n/auspex/s10/chip/euterpe
/n/auspex/s10/chip/euterpe/tools/bin/gastatus -sp gards/hc0-pass1) || (mv gards/hc0-
pass1.nof gards/hc0-pass1.nof.ERROR; rm -f hc0-pass1.nof; false)

```

Requires a minimum license of xgplace1_3 or gards1_3 .

Applicable licenses available at your installation :

gardsconfig_3

94/09/20 12:42:06 Check out of a license failed.

94/09/20 12:42:06 Will attempt again to check out a license in 2 minutes...

94/09/20 12:44:06 Now attempting to check out a license.

Checked out one user token of a gardsconfig_3 license.

GARDS GPLACE 7.119 -- General Placer

Copyright (c) 1994 SILVAR-LISCO. All rights reserved.

Design: hc0-pass1 Started at: 94/09/20 12:42:05

GPLACE Version 7.1.19 of November 22, 1993

No component hierarchy found; select by hierarchy disabled.

Loading components...

Loading nets...

Loading logical types...
Processing physical types...
Loading cell_types...
Creating net-comp xref table...

Terminated at : 94/09/20 12:49:35
Elapsed CPU time : 0 Hrs 3 Mins 41 Secs
Elapsed wall clock time : 0 Hrs 7 Mins 30 Secs
rm -f gards/gplace.nic
/n/auspex/s10/chip/euterpe/tools/bin/gasavepins gards/hc0-pass1.dff
Updating: gards/hc0-pass1.dff
gmake[2]: *** [gars/hc0-pass1.nof] Segmentation fault (core dumped)
gmake[2]: Leaving directory
~/N/auspex/root/s10/chip/euterpe/verilog/bsrc/hc'
gmake[1]: *** [hc0.short.nets] Error 1
gmake[1]: Leaving directory
~/N/auspex/root/s10/chip/euterpe/verilog/bsrc/hc'
gmake: *** [hc0gars] Error 1
[finished at Tue Sep 20 12:49:40 PDT 1994 -- exit status 0]

From: lisa
Sent: Tuesday, September 20, 1994 3:28 PM
To: 'Gregg Kellogg'
Subject: Re: 1128ba problems in simulator

Try ~lisa/bin/sgi5/tgdb; it should do better. Let me know if you need terp or uvterp; I have fixed ones of those, also.

lisa

.

From: Lisa Robinson [lisar@nosferatu]
Sent: Tuesday, September 20, 1994 3:31 PM
To: 'jeffm@nosferatu'
Cc: 'mws@nosferatu'; 'woody@nosferatu'; 'billz@nosferatu'; 'tbr@nosferatu'
Subject: expctest

xcorrupt.

Dump in /n/nosferatu/s1/euterpe/verilog/bsrc/expctest.

Lisa R.

From: lisa
Sent: Tuesday, September 20, 1994 3:53 PM
To: 'software-checkins-dist'
Subject: gnu-tools/sim/terp simgdb.c

Update of /p/cvsroot/gnu-tools/sim/terp
In directory calliope:/N/hyperion/root/s1/lisa/gnu-tools/sim/terp

Modified Files:
 simgdb.c
Log Message:

Removed superfluous return.

.

From: Jay Tomlinson [woody@melpomene]
Sent: Tuesday, September 20, 1994 5:04 PM
To: 'Lisa Robinson'
Cc: 'tbr@nosferatu'; 'billz@nosferatu'; 'mws@nosferatu'; 'jeffm@nosferatu'
Subject: gtlbaccess1

Lisa Robinson wrote (on Mon Sep 19):

Dump in /n/rhodan/s3/euterpe/verilog/bsrc/gtlbaccess1.*

Lisa R.

Lisa,

Please re-run this with DUMPSTART=9000. I think the problem is in nb (please dump all the way down). It looks like the store request is written into the array and overwritten before it can be read out. Just in case please also dump lt, gt, and uu. I suspect that actually multiple requests get overwritten but the actual test failure is the first one that I saw.

thanks,

Jay

From: lisa
Sent: Tuesday, September 20, 1994 6:21 PM
To: 'software-checkins-dist'
Subject: gnu-tools/sim/terp events.c execloop.c siminit.c

Update of /p/cvsroot/gnu-tools/sim/terp
In directory calliope:/N/hyperion/root/sl/lisa/gnu-tools/sim/terp

Modified Files:
 events.c execloop.c siminit.c
Log Message:

Keep track of how many threads we "stop" when idling; don't let all of the cylinders get stopped.

.

From: tbr
Sent: Tuesday, September 20, 1994 6:39 PM
To: 'vanthof'
Subject: pest
Follow Up Flag: Follow up
Flag Status: Red

Is it there yet? Just got:

tbr@staypuft ~/euterpe/verilog/bsrc/io 475 % pest

Running pest (Path ESTimator) compiled on Tue Sep 20 23:26:51 GMT 1994

Processing a: Mobimos, Flop/Latch design

path -> xbffedh8s 2.0 xbbufdh8s .25 xbmux5dh8s .25 xbmuxff2dh24s

SetSwingType: WARNING! Unknown swing xbffedh at line -1

Invalid first gate xbffedh8s. Either specify a correct gate or swing/power level: xbffdh12s || h12s

path ->

Tim

```
Tue Sep 20 20:19:26 PDT 1994 (geert Tue, 20 Sep 1994 20:19:02 -0700)
euterpe/verilog/bsrc/cc
[Release BOM (V10.0) in euterpe/verilog/bsrc/cc (Tue Sep 20 20:19:26 PDT 1994)]
```

9.1	.checkoutrc	(No)
1.6	Makefile	(1.5)
1.11	cc.V	(1.9)
1.3	cc.ut	(1.2)
5.7	cc_control.pim	(5.6)
1.3	cccounter.pla	
1.3	ccdecode.pla	
1.2	ccinprog.pla	
4.2	ccnbgo.Veqn	(4.1)
1.5	cctester.V	(1.3)
1.1	cctester.h	
5.4	genpim.pl	(5.3)
5.3	pimlib.pl	(5.2)
5.1	power.tab.local	

Exhibit C6

```

-y /n/auspex/s10/chip/euterpe/proteus/verilog/mlib
+libext+.v -y /n/auspex/s10/chip/euterpe/proteus/verilog/dxlib -y
/n/auspex/s10/chip/euterpe/proteus/verilog/dclib -y
/n/auspex/s10/chip/euterpe/proteus/verilog/delib
1 compilation error
V2E 1.0a Sep 20, 1994 20:17:16
* Copyright Cadence Design Systems Inc. 1990. *
* All Rights Reserved. Licensed Software. *
* Confidential and proprietary information which is the *
* property of Cadence Design Systems Inc. *
Compiling source file "cc.v"
Scanning library directory "."
Scanning library directory
"/n/auspex/s10/chip/euterpe/proteus/verilog/mlib"
Scanning library directory
"/n/auspex/s10/chip/euterpe/proteus/verilog/dxlib"
Warning! library directory
"/n/auspex/s10/chip/euterpe/proteus/verilog/dclib" was specified but not needed.
Warning! library directory
"/n/auspex/s10/chip/euterpe/proteus/verilog/delib" was specified but not needed.
"cc.v", 114: too many module port connections
End of V2E 1.0a Sep 20, 1994 20:17:22
gmake[1]: *** [cc.v2e] Error 1
gmake[1]: Leaving directory
~/N/auspex/root/s10/chip/euterpe/verilog/bsrc/cc'
gmake: *** [ccgards] Error 1
[finished at Tue Sep 20 20:20:48 PDT 1994 -- exit status 0]

```

From: Buffalo Chip [chip@ghidra]
Sent: Tuesday, September 20, 1994 10:38 PM
To: 'geert@ghidra'
Subject: output of euterpe/verilog/bsrc/cj/.checkoutrc

The output from euterpe/verilog/bsrc/cj/.checkoutrc is 176k, so it is not included in this mail message. Instead, check the file

/n/tmp/chiplog/geert.ghidra.7738.euterpe-verilog-bsrc-cj

(which is accessible from all machines). This file will disappear in about 5 days.

By the way, the exit status returned by .checkoutrc was 0.

.

From: Geert Rosseel [geert@ambiorix]
Sent: Tuesday, September 20, 1994 10:49 PM
To: 'agc@ambiorix'; 'tbr@ambiorix'
Subject: cc not working in /u/chip

I ran cc in /u/chip and I got :

```
CHIPROOT=/n/auspex/s10/chip/euterpe /n/auspex/s10/chip/euterpe/tools/bin/v2e -host st
aypuft cc.v -o cc.v2e -l cc.v2e.log -y . -y /n/auspex/s10/chip/euterpe/proteus/verilo
g/mlib +libext+.v -y /n/auspex/s10/chip/euterpe/proteus/verilog/dxlib -y /n/auspex/s1
0/chip/euterpe/proteus/verilog/dclib -y /n/auspex/s10/chip/euterpe/proteus/verilog/de
lib
l compilation error
V2E 1.0a Sep 20, 1994 20:17:16
* Copyright Cadence Design Systems Inc. 1990. *
* All Rights Reserved. Licensed Software. *
* Confidential and proprietary information which is the *
* property of Cadence Design Systems Inc. *
Compiling source file "cc.v"
Scanning library directory ""
Scanning library directory "/n/auspex/s10/chip/euterpe/proteus/verilog/mlib"
Scanning library directory "/n/auspex/s10/chip/euterpe/proteus/verilog/dxlib"
Warning! library directory "/n/auspex/s10/chip/euterpe/proteus/verilog/dclib" was spe
cified but not needed.
Warning! library directory "/n/auspex/s10/chip/euterpe/proteus/verilog/delib" was spe
cified but not needed.
"cc.v", 114: too many module port connections
End of V2E 1.0a Sep 20, 1994 20:17:22
gmake[1]: *** [cc.v2e] Error 1
```

Geert

.

From: tbr
Sent: Tuesday, September 20, 1994 11:05 PM
To: 'Geert Rosseele'
Cc: 'agc@ambiorix'; 'billz'
Subject: cc not working in /u/chip
Follow Up Flag: Follow up
Flag Status: Red

Geert Rosseele wrote (on Tue Sep 20):

I ran cc in /u/chip and I got :

```
CHIPROOT=/n/auspex/s10/chip/euterpe /n/auspex/s10/chip/euterpe/tools/bin/v2e -host st
aypuft cc.v -o cc.v2e -l cc.v2e.log -y . -y /n/auspex/s10/chip/euterpe/proteus/verilo
g/mlib +libext+.v -y /n/auspex/s10/chip/euterpe/proteus/verilog/dxlib -y /n/auspex/s1
0/chip/euterpe/proteus/verilog/dclib -y /n/auspex/s10/chip/euterpe/proteus/verilog/de
lib
l compilation error
V2E 1.0a Sep 20, 1994 20:17:16
* Copyright Cadence Design Systems Inc. 1990. *
* All Rights Reserved. Licensed Software. *
* Confidential and proprietary information which is the *
* property of Cadence Design Systems Inc. *
Compiling source file "cc.v"
Scanning library directory ":"
Scanning library directory "/n/auspex/s10/chip/euterpe/proteus/verilog/mlib"
Scanning library directory "/n/auspex/s10/chip/euterpe/proteus/verilog/dxlib"
Warning! library directory "/n/auspex/s10/chip/euterpe/proteus/verilog/dclib" was spe
cified but not needed.
Warning! library directory "/n/auspex/s10/chip/euterpe/proteus/verilog/delib" was spe
cified but not needed.
"cc.v", 114: too many module port connections
End of V2E 1.0a Sep 20, 1994 20:17:22
gmake[1]: *** [cc.v2e] Error 1
```

Geert

Which BOM are you working off. There is a lot of stuff in flux in cc.
As far as I know BOM 9.0 compiles OK.

Tim

From: Tim B. Robinson [tbr@aphrodite]
Sent: Tuesday, September 20, 1994 11:05 PM
To: 'Geert Rosseel'
Cc: 'aggc@ambiorix'; 'billz@aphrodite'
Subject: cc not working in /u/chip

Geert Rosseel wrote (on Tue Sep 20):

I ran cc in /u/chip and I got :

```
CHIPROOT=/n/auspex/s10/chip/euterpe
/n/auspex/s10/chip/euterpe/tools/bin/v2e -host st
aypuft cc.v -o cc.v2e -l cc.v2e.log -y . -y /n/auspex/s10/chip/euterpe/proteus/verilo
g/mlib +libext+.v -y /n/auspex/s10/chip/euterpe/proteus/verilog/dxlib
-y /n/auspex/s1
0/chip/euterpe/proteus/verilog/dclib -y /n/auspex/s10/chip/euterpe/proteus/verilog/de
lib
1 compilation error
V2E 1.0a Sep 20, 1994 20:17:16
* Copyright Cadence Design Systems Inc. 1990. *
* All Rights Reserved. Licensed Software. *
* Confidential and proprietary information which is the *
* property of Cadence Design Systems Inc. *
Compiling source file "cc.v"
Scanning library directory "."
Scanning library directory
"/n/auspex/s10/chip/euterpe/proteus/verilog/mlib"
Scanning library directory
"/n/auspex/s10/chip/euterpe/proteus/verilog/dxlib"
Warning! library directory
"/n/auspex/s10/chip/euterpe/proteus/verilog/dclib" was spe
cified but not needed.
Warning! library directory
"/n/auspex/s10/chip/euterpe/proteus/verilog/delib" was spe
cified but not needed.
"cc.v", 114: too many module port connections
End of V2E 1.0a Sep 20, 1994 20:17:22
gmake[1]: *** [cc.v2e] Error 1
```

Geert

Which BOM are you working off. There is a lot of stuff in flux in cc.
As far as I know BOM 9.0 compiles OK.

Tim

From: Lisa Robinson [lisar@nosferatu]
Sent: Tuesday, September 20, 1994 11:10 PM
To: 'woody@nosferatu'; 'jeffm@nosferatu'
Cc: 'mws@nosferatu'; 'billz@nosferatu'; 'tbr@nosferatu'
Subject: gtlibaccess1

New dump as requested (at long last!)
/n/rhodan/s3/euterpe/verilog/bsrc/gtlibaccess1.*

Lisa R.

.

From: Jay Tomlinson [woody@demeter]
Sent: Tuesday, September 20, 1994 11:33 PM
To: 'Lisa Robinson'
Cc: 'billz@nosferatu'; 'jeffm@nosferatu'; 'mws@nosferatu'; 'tbr@nosferatu'
Subject: gtlbaccess1

I suggest billz look at this, because I think the problem is in nb.

Lisa Robinson wrote (on Tue Sep 20):

New dump as requested (at long last!)
/n/rhodan/s3/euterpe/verilog/bsrc/gtlbaccess1.*

Lisa R.

.

From: Lisa Robinson [lisar@nosferatu]
Sent: Wednesday, September 21, 1994 12:29 AM
To: 'jeffm@nosferatu'
Cc: 'mws@nosferatu'; 'woody@nosferatu'; 'billz@nosferatu'; 'tbr@nosferatu'
Subject: expctest

New expctest dump as requested (I may not have dumped all you need)

/n/rhodan/s3/euterpe/verilog/bsrc/expctest.*

Lisa R.

.

From: tbr
Sent: Wednesday, September 21, 1994 12:53 AM
To: 'vanthof'
Cc: 'ericm'; 'gmo'; 'brendan'
Subject: topt
Follow Up Flag: Follow up
Flag Status: Red

Is there any possibility that when topt reads in a strength file from an earlier run it somehow touches the file and so changes the modified date?

I'm still trying to get to the bottom of the erratic Makefile behavior and I have a log from a 'gmake -d' which suggests that in pass 1, it makes the cj-pass1.strength file, then makes the gards/cj-pass1macros.pld file as I would expect. However when it came to the recursive invocation of gmake to run pass 2 it reported that the cj-pass1.strength file was **newer** than the gards/cj-pass1macros.pdl file and so it went back and ran a bunch of pass 1 stuff again.

For reference the log is in ~tbr/euterpe/verilog/bsrc/cj/makerrrs

Tim

.

From: tbr
Sent: Wednesday, September 21, 1994 12:14 PM
To: 'tom'
Subject: /u/chip
Follow Up Flag: Follow up
Flag Status: Red

I have removed all the intermediate .edif and .v2e files in euterpe in /u/chip. We are back to 44MB and the newly release Makefiles will now dump these in the gards subdirs.

Tim

.

From: Tom Laidig [tom@clio]
Sent: Wednesday, September 21, 1994 12:29 PM
To: 'Tim B. Robinson'
Subject: Re: /u/chip

Tim B. Robinson writes:

|
| I have removed all the intermediate .edif and .v2e files in euterpe in
| /u/chip. We are back to 44MB and the newly release Makefiles will now
| dump these in the gards subdirs.

Great! I still think it would be wise to open up more free space, but
this cuts down the urgency a bit.

--

Tom L

.

From: tbr
Sent: Wednesday, September 21, 1994 1:12 PM
To: 'Tom Laidig'
Subject: Re: /u/chip
Follow Up Flag: Follow up
Flag Status: Red

Tom Laidig wrote (on Wed Sep 21):

Tim B. Robinson writes:

|
|I have removed all the intermediate .edif and .v2e files in euterpe in
|/u/chip. We are back to 44MB and the newly release Makefiles will now
|dump these in the gards subdirs.

Great! I still think it would be wise to open up more free space, but
this cuts down the urgency a bit.

There may be other derived stuff that can go there too, but it's
likely to be small.

Tim

From: tbe@microunity.com
Sent: Wednesday, September 21, 1994 2:08 PM
To: 'Wayne Freitas'
Cc: 'abbott@microunity.com'; 'noel@microunity.com'; 'tbe@microunity.com';
'hchu@microunity.com'; 'hestia@microunity.com'; 'h@microunity.com'
Subject: Re: Electrical system definition

On September 20, Wayne Freitas wrote:

>This is the list of descerepencies primarily between the MediaComputer
>Technical Summary and the Digital Terminal specification. I need to
>know what items are correct for verifying Hestia. So if the individuals
>listed below could provide their comments to help straighten this list
>out I would greatly appreciate it.

>
>Thanks,
>
>Wayne
>
>snip<
>
> HD - Operating Temperature 0 to 50 deg C
> MC - 0 to 50 deg C derated to 40 deg
> between 2,000 and 10,000 ft.
> DT - 0 to 50 deg C
>
>tbe/Herman, could you comment on these?
>

All of the above are out of date; the HD and DT specs don't deal with altitude in combination with temperature and the MC spec should only go to 7000 feet. Since that is our own spec, I suggest we change it as follows for the first units.

Because of the power growth seen since March, we have been saying that the first trial units will meet 0 to 40 C up to 7000 feet altitude. Until we build and thermally test functioning units, we should not sign up to a wider temperature range. It seems too risky to me to gaurantee performance above this level without survey test data. I suggest the 50 C spec should be deferred for now.

I think that when the final (functioning) Calliope and Euterpe power dissipation is known and the corresponding performance and temperature rises are measured is the time to derive prudent environmental specs, negotiate them with our customers, and make any necessary design mods to meet same.

-Tom

Tom Eich
MicroUnity Systems Engineering, Inc.
255 Caspian Dr. Sunnyvale, CA 94089
(408)734-8100, (408)734-8136 fax

tbe@microunity.com

.

From: Richard Dickson [dickson@ghidra]
Sent: Wednesday, September 21, 1994 6:32 PM
To: 'tbr@ghidra'
Subject: csyn

tim

it only 1/2 Mbyte now. i'll go thru it tonite and digest it.

-rw-r--r-- 1 dickson 435456 Sep 21 16:27 tbr_euterpe-pass1.csyn

dickson

.

From: Lisa Robinson [lisar@rhodan]
Sent: Wednesday, September 21, 1994 6:35 PM
To: 'billz@rhodan'; 'woody@rhodan'
Cc: 'dickson@rhodan'; 'jeffm@rhodan'; 'mws@rhodan'; 'tbr@rhodan'
Subject: knobreallyeasy

This just does a l64li of outlet 24 then stores it back. The correct value is committed to the register file e0e0e0e0e0e0e0 but then the test goes to x.

Dump in /n/rhodan/s3/eutercp/verilog/bsrc/knobreallyeasy.*

Lisa R.

From: vant [vanthof@hestia]
Sent: Wednesday, September 21, 1994 7:18 PM
To: 'Eldred Fellas'
Cc: 'Dave Van't Hof'; 'Geert Rosseel'; 'Mark Hofmann'
Subject: gtlb waffles.

Eldred

I've completed the generation of the waffles for the gtlb. Can you copy the file:

/u/vanthof/compass/mobi/euterpe/gtlb_waf.ly

to your area, then run drc's? if it passes, or is easily fixed, then force the chekin of this cell to proteus.

Thanks,
Dave

--

Dave Van't Hof vanthof@microunity.com MicroUnity Systems Engineering,
Inc.

"What rolls down stairs, alone or in pairs, rolls over the neighbor's dog?"

What's great for a snack and fits on your back? It's log, log, log!"

LOG from BLAMMO! (tm) All kids love Log! #include

<std_disclaim.h>

.

From: tbr
Sent: Wednesday, September 21, 1994 7:57 PM
To: 'Richard Dickson'
Subject: csyn
Follow Up Flag: Follow up
Flag Status: Red

Richard Dickson wrote (on Wed Sep 21):

tim

it only 1/2 Mbyte now. i'll go thru it tonite and digest it.

-rw-r--r-- 1 dickson 435456 Sep 21 16:27 tbr_euterpe-pass1.csyn

Progress at least. I expect most of it is still the 1p xlu outputs.

Tim

From: Eric Murray [ericm@microunity.com]
Sent: Wednesday, September 21, 1994 8:18 PM
To: 'Tim B. Robinson'
Cc: 'hopper@microunity.com'; 'vanthof@microunity.com'; 'brianl@microunity.com';
'geert@microunity.com'; 'sysadmin@microunity.com'
Subject: Re: Ahrrghh!!! missing data

Tim B. Robinson wrote:

>
>
> I think this is a network glitch. On gammora a build in /u/chip just
> died because topt crashed with:
>
>
> ERROR! Could not stat
> /n/auspex/s10/chip/euterpe/proteus/custom/caps/cap.lib
>

yea, i just had a network problem. actually about three different problems. i have them
straightened out now, though i'll need to make a replacement cable tomorrow.

--

ericm ericm@microunity.com

.

From: tbr
Sent: Wednesday, September 21, 1994 9:05 PM
To: 'hopper'; 'vanthof'; 'brian'
Cc: 'geert'; 'sysadmin'
Subject: Ahrrghh!!! missing data
Follow Up Flag: Follow up
Flag Status: Red

I think this is a network glitch. On gammora a build in /u/chip just died because topt crashed with:

ERROR! Could not stat /n/auspex/s10/chip/euterpe/proteus/custom/caps/cap.lib

However:

```
tbr@gamorra ~/euterpe/verilog/bsrc/cj 603 % ls -ls /n/auspex/s10/chip/euterpe/proteus/cu  
stom/caps/cap.lib  
 33 -rw-r--r-- 1 chip    33557 Sep 21 10:20 /n/auspex/s10/chip/euterpe/proteus/custom/caps/cap.lib
```

Tim

From: Tim B. Robinson [tbr@aphrodite]
Sent: Wednesday, September 21, 1994 9:05 PM
To: 'hopper@aphrodite'; 'vanthof@aphrodite'; 'brianl@aphrodite'
Cc: 'geert@aphrodite'; 'sysadmin@aphrodite'
Subject: Ahrrghh!!! missing data

I think this is a network glitch. On gammora a build in /u/chip just died because topt crashed with:

ERROR! Could not stat
/n/auspex/s10/chip/euterpe/proteus/custom/caps/cap.lib

However:

```
tbr@gamorra ~/euterpe/verilog/bsrc/cj 603 % ls -ls -ls /n/auspex/s10/chip/euterpe/proteus/cu
stom/caps/cap.lib
 33 -rw-r--r--  1 chip          33557 Sep 21 10:20
/n/auspex/s10/chip/euterpe/proteus/custom/caps/cap.lib
```

Tim

.

From: tbr
Sent: Wednesday, September 21, 1994 9:07 PM
To: 'hopper'; 'sysadmin'
Cc: 'geert'; 'brianl'
Subject: Correction
Follow Up Flag: Follow up
Flag Status: Red

Sorry, the build that died was on staypuff. However, the file is visible there too now:

```
tbr@staypuff ~/euterpe/verilog/bsrc/cdio 536 % ls -ls /n/auspex/s10/chip/euterpe/proteus/custom/caps/cap.lib
33 -rw-r--r-- 1 chip 33557 Sep 21 10:20 /n/auspex/s10/chip/euterpe/proteus/custom/caps/cap.lib
```

Tim

From: Tim B. Robinson [tbr@aphrodite]
Sent: Wednesday, September 21, 1994 9:07 PM
To: 'hopper@aphrodite'; 'sysadmin@aphrodite'
Cc: 'geert@aphrodite'; 'brianl@aphrodite'
Subject: Correction

Sorry, the build that died was on staypuft. However, the file is visible there too now:

```
tbr@staypuft ~/euterpe/verilog/bsrc/cdio 536 % ls -ls  
/n/auspex/s10/chip/euterpe/proteus/custom/caps/cap.lib  
33 -rw-r--r-- 1 chip 33557 Sep 21 10:20  
/n/auspex/s10/chip/euterpe/proteus/custom/caps/cap.lib
```

Tim

.

From: tbr
Sent: Wednesday, September 21, 1994 9:28 PM
To: 'Eric Murray'
Cc: 'brianl@MicroUnity.com'; 'geert@MicroUnity.com'; 'hopper@MicroUnity.com'; 'sysadmin@MicroUnity.com'; 'vanthof@MicroUnity.com'
Subject: Re: Ahrrghh!!! missing data
Follow Up Flag: Follow up
Flag Status: Red

Eric Murray wrote (on Wed Sep 21):

Tim B. Robinson wrote:

>
>
> I think this is a network glitch. On gammora a build in /u/chip just
> died because topt crashed with:
>
>
> ERROR! Could not stat /n/auspex/s10/chip/euterpe/proteus/custom/caps/cap.lib
>

yea, i just had a network problem. actually about three different problems. i have them straightened out now, though i'll need to make a replacement cable tomorrow.

OK, I'll restart this lot and see if it fares any better.

Tim

From: Tim B. Robinson [tbr@aphrodite]
Sent: Wednesday, September 21, 1994 9:28 PM
To: 'Eric Murray'
Cc: 'brianl@microunity.com'; 'geert@microunity.com'; 'hopper@microunity.com';
'sysadmin@microunity.com'; 'vanthof@microunity.com'
Subject: Re: Ahrrghh!!! missing data

Eric Murray wrote (on Wed Sep 21):

Tim B. Robinson wrote:
>
>
> I think this is a network glitch. On gammora a build in /u/chip just
> died because topt crashed with:
>
>
> ERROR! Could not stat
/n/auspex/s10/chip/euterpe/proteus/custom/caps/cap.lib
>

yea, i just had a network problem. actually about three different
problems. i have them straightened out now, though i'll
need to make a replacement cable tomorrow.

OK, I'll restart this lot and see if it fares any better.

Tim

.

From: Lisa Robinson [lisar@nosferatu]
Sent: Wednesday, September 21, 1994 11:17 PM
To: 'jeffm@nosferatu'; 'billz@nosferatu'
Cc: 'tbr@nosferatu'
Subject: dramload

I can't seem to reproduce this failure in verilog. I seem to have managed to get the model to read the .in files (which I hand split) but euterpe just reads x out of them.

The failure in zycad land was that a 128 bit load from dram seem to result in an unexpected extra commit to the register file of the octlet jumbled correct data. I'll re-run with some extra signals dumped.

Jeff your dramsplit splits into 2 files 32 bits wide shouldn't it be 16 bits wide?

This is what I get with 32 bit wide data

Warning! Too many digits in "dramh.in" at line 1 [Verilog-TMDAL]
"dv_euterpe_wrap.v", 291: \$readmemh("dramh.in",
sdram1.memory);

Lisa R.

.

From: Jay Tomlinson [woody@demeter]
Sent: Thursday, September 22, 1994 12:20 AM
To: 'tbr@demeter'
Subject: Makefile.?

Tim,

I do not know if this has anything to do with any of the Makefiles that you have been changing, but when I try to make lt-pass1.size I get the following error:

```
Writing output to gards/lt.v2e ....
0 warnings 0 errors
End of V2E 1.0a Sep 21, 1994 22:09:06
Wed Sep 21 22:12:56 PDT 1994
CHIPROOT=/n/auspex/s20/woody/chip/euterpe /n/auspex/s20/woody/chip/euterpe/tools
/bin/emerge -f -R -p emerge.tab -c gards/lt.v2e -o gards/lt.edif -O gards/lt.emer
ge.log
```

Running emerge compiled on Wed Sep 21 23:46:30 GMT 1994

```
Consuming edif file gards/lt.v2e
Found edif structure: LT_46_V2E
```

ERROR! Multiple Design statements in edif.
Please fix before continuing.

```
rhodan:[~/chip/euterpe/verilog/bsrc/lt]$ grep -i design gards/lt.v2e
(author "Cadence Design Systems Inc.")
(rename DESIGN_LIB "DESIGN_LIB")
(design
(libraryRef DESIGN_LIB)))
(design
(libraryRef DESIGN_LIB))))
rhodan:[~/chip/euterpe/verilog/bsrc/lt]$
```

Funny thing is it work a few minutes ago?! FYI, I commented out the upper bits of the tag and it saved about 1500 atoms.

jay

.

From: tbr
Sent: Thursday, September 22, 1994 12:24 AM
To: 'Jay Tomlinson'
Subject: Makefile.?
Follow Up Flag: Follow up
Flag Status: Red

Jay Tomlinson wrote (on Wed Sep 21):

Tim,

I do not know if this has anything to do with any of the Makefiles that you have been changing, but when I try to make lt-pass1.size I get the following error:

```
Writing output to gards/lt.v2e ....
0 warnings 0 errors
End of V2E 1.0a Sep 21, 1994 22:09:06
Wed Sep 21 22:12:56 PDT 1994
CHIPROOT=/n/auspex/s20/woody/chip/euterpe /n/auspex/s20/woody/chip/euterpe/tools
/bin/emerge -f -R -p emerge.tab -e gards/lt.v2e -o gards/lt.edif -O gards/lt.emer
rge.log
```

Running emerge compiled on Wed Sep 21 23:46:30 GMT 1994

```
Consuming edif file gards/lt.v2e
Found edif structure: LT_46_V2E
```

ERROR! Multiple Design statements in edif.
Please fix before continuing.

```
rhodan:[~/chip/euterpe/verilog/bsrc/lt]$ grep -i design gards/lt.v2e
(author "Cadence Design Systems Inc.")
(rename DESIGN_LIB "DESIGN_LIB")
(design
(libraryRef DESIGN_LIB)))
(design
(libraryRef DESIGN_LIB)))
rhodan:[~/chip/euterpe/verilog/bsrc/lt]$
```

Dunno what that could be. Did v2e report more than one highest level modules?

Funny thing is it work a few minutes ago?! FYI, I commented out the upper bits of the tag and it saved about 1500 atoms.

With regard to all the makefile changes, I suggest you pick up the latest Makefile.share. Then you can delete the local v2e rule in your lt Makefile as there is now a generic one in Makefile.share.

I have been building about 6 sections in /u/chip and I have not seen any trouble.

Tim

.

From: Mark Hofmann [hopper@cyclops]
Sent: Thursday, September 22, 1994 5:11 AM
To: 'Richard Dickson'
Cc: 'Tim B. Robinson'
Subject: Re: core dump

Richard Dickson writes:
mark,

at dickson/euterpe/verilog/bsrc/mc theres a core file.
aaa is my log file.

```
/n/rama/s5/dickson/euterpe/tools/bin/pim2pif.ex: (2014, 35) to (2816, 479) [401
by 148 ECL atoms]
/n/rama/s5/dickson/euterpe/tools/bin/pim2pif.ex: 21003 ECL atoms placed in 59348
[-3108 obstructions] atom area [37.35% dense]
#pim2pif.ex Version 0.2.15 Wed Sep 21 10:07:08 PDT 1994
/n/rama/s5/dickson/euterpe/tools/bin/pifpack: Packing left edge...
Segmentation fault (core dumped)
gmake[2]: *** [gards/mc-iter.pif] Error 11
gmake[2]: Leaving directory '/N/rama/root/s5/dickson/euterpe/verilog/bsrc/mc'
gmake[1]: *** [gards/mc-iter] Error 1
gmake[1]: Leaving directory '/N/rama/root/s5/dickson/euterpe/verilog/bsrc/mc'
gmake: *** [mcgards] Error 1
```

Rich-

This is bizarre, the core file `_is_` from `pim2pif.ex`. However I just re-ran
with what I think is your exact data and everything went fine. Could you
try a re-run?

-thanks,
hopper

.

From: Geert Rosseel [geert@ambiorix]
Sent: Thursday, September 22, 1994 12:32 PM
To: 'agc@ambiorix'; 'billz@ambiorix'; 'dickson@ambiorix'; 'geert@ambiorix'; 'mws@ambiorix';
'tbr@ambiorix'; 'vo@ambiorix'; 'woody@ambiorix'
Subject: Latest routing results

If anybody wants to look at the latest routing results, they are stored
in ~geert/chip/euterpe/verilog/bsrc/gards.save

Geert

From: Richard Dickson [dickson@demeter]
Sent: Thursday, September 22, 1994 12:35 PM
To: 'geert@demeter'
Subject: routed blocks

geert,

mst and gf are ready. mc should be ready soon. mc core dumped on me last nite but its running now. should be done in a couple of hours.
its at dickson/euterpe/verilog/bsrc/mst and gf

dickson`

□

From: Mark Hofmann [hopper@cyclops]
Sent: Thursday, September 22, 1994 12:42 PM
To: 'Geert Rosseel'; 'Tim B. Robinson'
Subject: output of euterpe/verilog/bsrc/io/.checkoutrc (fwd)

Could you look in to this?

-thanks.
hopper

Buffalo Chip writes:

From: chip@tomato Thu Sep 22 17:36:21 1994
Date: Thu, 22 Sep 1994 17:36:18 -0700
From: chip@tomato (Buffalo Chip)
Message-Id: <199409230036.RAA28028@tomato.microunity.com>
To: hopper@tomato
Subject: output of euterpe/verilog/bsrc/io/.checkoutrc

Thu Sep 22 17:34:42 PDT 1994 (hopper Thu, 22 Sep 1994 17:34:19 -0700)
euterpe/verilog/bsrc/io
[Release BOM (V11.0) in euterpe/verilog/bsrc/io (Thu Sep 22 17:34:43 PDT 1994)]

```
Dir          euterpe/verilog/bsrc/io          BOM
11.0
  9.1      .checkoutrc
  1.9      Makefile
  9.1      clean-request
  8.1      genpim0.pl
  8.4      genpim1.pl
(8.3)
  7.4      io_control.pim
  8.2      io_control_2.pim
  6.1      io_ififo.V
  6.1      io_iphase.Veqn
  6.1      io_ofifo.V
  6.1      io_ophase.Veqn
  6.1      io_scioff_6.V
  6.1      io_scioff_9.V
  3.1      ioCount.pla
  3.2      iodrive.V
  3.1      iofs.Veqn
  3.2      iorate.V
  3.4      iosync.V
  4.6      pimlib.pl
  7.1      power.tab.local
====> running euterpe/verilog/bsrc/io/.checkoutrc (Thu Sep 22 17:34:50 PDT 1994) <===
gmake: `clean' is up to date.
gmake[1]: *** [gards/io0-iter] Error 1
gmake: *** [io0gards] Error 1
#
# turn off pgroute
#
[ -f nopgroute ] || touch nopgroute
#
# use padtiles
#
[ -f usepadtiles ] || touch usepadtiles
#
# use pifpack
#
[ -f usepifpack ] || touch usepifpack
#
# insert an instance of the clock tree
#
```

```

[ -f addclock ] || touch addclock
#
# Disable old dcell placement obstruction
#
[ -f gards/noobs ] || touch gards/noobs
#
# Now do it . . .
#
gmake GARDS_DISPLAY=clio:0.0 gards/io0-iter
gmake[1]: Entering directory
~/N/auspex/root/s10/chip/euterpe/verilog/bsrc/io'
#
# Final report
#   Done if no timing errors
#   Iterate if only correctable timing errors
#   Give up if uncorrectable timing errors
#
CHIPROOT=/n/auspex/s10/chip/euterpe
/n/auspex/s10/chip/euterpe/tools/bin/topt -p
/n/auspex/s10/chip/euterpe/proteus/misc/power.tab -p power.tab.local -h
/n/auspex/s10/chip/euterpe/proteus/leafgen/dclload/dclload.lib -h
/n/auspex/s10/chip/euterpe/proteus/e      xlax/dclload/dclload.lib -h
/n/auspex/s10/chip/euterpe/proteus/custom/dclload/dclload.lib -g
/n/auspex/s10/chip/euterpe/proteus/leafgen/toptList -g
/n/auspex/s10/chip/euterpe/proteus/exlax/toptList -g
/n/auspex/s10/chip/euterpe/proteus/custom/toptList \
-A /n/auspex/s10/chip/euterpe/proteus/leafgen/caps/cap.lib -A
/n/auspex/s10/chip/euterpe/proteus/exlax/caps/cap.lib -A
/n/auspex/s10/chip/euterpe/proteus/custom/caps/cap.lib -H
/n/auspex/s10/chip/euterpe/proteus/leafgen/time/tim.lib -H
/n/auspex/s10/chip      /euterpe/proteus/custom/time/tim.lib -H
/n/auspex/s10/chip/euterpe/proteus/exlax/time/tim.lib \
-l 926 \
-e gards/io0.edif -K io0-base.strength -L io0-base.netcap \
-s gards/io0-final.stat -O gards/io0-final.topt.log \
-z 2 -M mobimos -R -t 50 -b 10 -a 24 -S; \
case $? in \
0) echo -n '**** converged in 0 iteration'; \
    cp gards/ordered.all.nets gards/io0.ordered.all.nets; \
    if (expr 0 = 1 > /dev/null) then \
        echo ' ****'; \
    else \
        echo 's ****'; \
    fi; \
    touch gards/io0-iter;; \
1) if (expr 0 \> 8 > /dev/null) then \
    exit 1; \
    else \
        cp io0-base.pim io0-iter.pim; \
        gmake GARDS_DISPLAY=clio:0.0 CYCLETIME=895 gards/io0-iter.garout.lis || exit
1; \
        cp gards/ordered.all.nets gards/io0.ordered.all.nets; \
        cp io0-iter.netcap io0-base.netcap; \
        cp io0-iter.strength io0-base.strength; \
        gmake GARDS_DISPLAY=clio:0.0 ITERATION=`expr 0 + 1` gards/io0-iter; \
    fi;; \
*) exit 1;; \
esac

```

Running topt (Power OPTimizer) compiled on Wed Sep 21 23:45:40 GMT 1994

```

Processing a: Mobimos, Flop/Latch design
Consuming edif file gards/io0.edif
Found edif structure: gards_47_io0_46.edif
Flattening edif;
IORATE already flat.
found 423 instances;      found 1073 nets in gards_47_io0_46.edif
Consuming power table information file

```

```

/n/auspex/s10/chip/euterpe/teus/misc/power.tab
Consuming power table information file power.tab.local
Reading Stats file
/n/auspex/s10/chip/euterpe/teus/leafgen/stats.ec1
Reading Stats file
/n/auspex/s10/chip/euterpe/teus/leafgen/stats.cmos
Reading Stats file
/n/auspex/s10/chip/euterpe/teus/exlax/stats.ea
Reading Stats file
/n/auspex/s10/chip/euterpe/teus/custom/stats.ec1
Reading Legal Cell List file
/n/auspex/s10/chip/euterpe/teus/leafgen/toptList
Reading Legal Cell List file
/n/auspex/s10/chip/euterpe/teus/exlax/toptList
ReadLegalCellFile: Warning! No atoms info for ealnf36s9x4a
Reading Legal Cell List file
/n/auspex/s10/chip/euterpe/teus/custom/toptList
Performing Edif Transformations...
Reading DC Loads file
/n/auspex/s10/chip/euterpe/teus/leafgen/dclload/dclload.lib
Reading DC Loads file
/n/auspex/s10/chip/euterpe/teus/exlax/dclload/dclload.lib
Reading DC Loads file
/n/auspex/s10/chip/euterpe/teus/custom/dclload/dclload.lib
Reading LPE extracted data from io0-base.netcap.

Reading pin cap values from
/n/auspex/s10/chip/euterpe/teus/leafgen/caps/cap.lib
Reading pin cap values from
/n/auspex/s10/chip/euterpe/teus/exlax/caps/cap.lib
Reading pin cap values from
/n/auspex/s10/chip/euterpe/teus/custom/caps/cap.lib
Status information in gards/io0-final.stat
Warning! Cell cgclockbias not on legal cell list.
Any gate in it's path is not AC power optimized
No swing calculations will be performed
Warning! Cell sccgdr not on legal cell list.
Any gate in it's path is not AC power optimized
No swing calculations will be performed
Pruning flattened network of unused instances... 0 pruned in 1
pass.
Checking/Setting swing values...
Found 5 Warnings! Please check stat file!

Reading Cap/Delay table file
/n/auspex/s10/chip/euterpe/teus/leafgen/time/tim.lib
Reading Cap/Delay table file
/n/auspex/s10/chip/euterpe/teus/custom/time/tim.lib
Warning! Cell cache at line 4 is not in legal cell list
Warning! Cell cahalf at line 10 is not in legal cell list
Warning! Cell cr at line 13 is not in legal cell list
Warning! Cell ctg at line 20 is not in legal cell list
Warning! Cell gtlb at line 23 is not in legal cell list
Warning! Cell sccgbfr0 at line 52 is not in legal cell list
Warning! Cell scsof3v3 at line 188 is not in legal cell list
Reading Cap/Delay table file
/n/auspex/s10/chip/euterpe/teus/exlax/time/tim.lib

Connecting floating differential inputs to net vref_0ph...
Connected 0 inputs to net vref_0ph...
Reading the drive strength file io0-base.strength and setting power levels
NOTE! Cell cgclockbias has strength of 0
DC Load checks only for cell(s):
eawwlvref56s7x4a eawwlvref20s10x1a eawwlvref16s2x4a xbc01df32s
xbc01df24s xbc01df16s xbc01df12s xbc01df8s xbc01df6s xbc01df4s
xbc01df2s xbc01 xbcmos2ecldf16s xbcmos2ecldf12s xbcmos2ecldf8s
xbcmos2ecldf4s xbcmos2ecldf2s xbcmos2ec1
Warning! No CKFI_AD1PH pin capacitance data for cgclockbias

```


Warning! No ckfi_ad0ph pin capacitance data for sccgdr
Warning! No ckfi_bd0ph pin capacitance data for sccgdr

Ignoring these nets:
PHI_B2P PHI_A2P vref_0ph

Optimizing power...

Iteration: 1

Path power optimizer

IntrinsicWarning: Warning! No clk_to_q flipflop fanin 1 delay for flipflop scsynchl1

NOTE: Cell scsynchl1 using 'intrinsic delay + .7RC'

calculations.

IntrinsicWarning: Warning! No setup gate fanin 1 delay for flipflop scsynchl1 for

input pin D0_AD0PF

IntrinsicWarning: Warning! No clk_to_q gate fanin 1 delay for gate xbcmos2ecldf2s for

input pin CIN_ABM

ERROR! 123 paths exceeded cycle time. Check status file.

DC Load Calculations

ERROR! 5 under-powered instances based on DC load.

Unpowered Instance check: 1 found.

Savings by squeezing out extra time = (2246 - 2246) = 0.00%

Change from original input power = (2246 - 2246) = 0.00%

NOTE: 773 unpowered nets.

Atoms:	count	atom	bjt	isrc	pld	clock
BJT Totals:	423	3311	6388	5118	4860	1868

Memory usage: 22.977MB

Exit code: 2 (Failed Max Timing)

gmake[1]: Leaving directory

~/N/auspex/root/s10/chip/euterpe/verilog/bsrc/io'

[finished at Thu Sep 22 17:36:18 PDT 1994 -- exit status 1]

-thanks,
hopper

thanks,
mark hofmann
hopper@microunity.com
408 734 8100

From: Herman Chu [hchu@phobos.microunity.com]
Sent: Thursday, September 22, 1994 1:19 PM
To: 'noel@phobos.microunity.com'; 'trancy@phobos.microunity.com'
Cc: 'hchu@phobos.microunity.com'; 'hestia@phobos.microunity.com';
'euterpe@phobos.microunity.com'
Subject: TAB Lead Steady-state Thermal Testing/Analysis

I have performed testing on the TAB leads in an isolated bare TAB frame, that is no die/ST, no PCB, and no heat sink attached. I tried to measure temperature as close to the powered leads as possible while minimizing the disturbance to the overall thermal characteristics of the TAB frame (The Uncertainty Principle). The current thermal and electrical test equipments that we have are not adequate for precise measurements for this

level of packaging test, nonetheless, with the limited time that I have for testing and evaluation, the results provided me with valuable ball park estimates of the thermal performance of the leads under intended operating

environment.

The lead temperature was not measured directly, therefore the lead temperature results presented below are based upon test results and analytical extrapolations.

2 cases were tested. The first case was tested with only 1 lead powered on, and in the seconde case 5 leads were powered on.

Results:

The estimated lead temperatures are presented in the following table:

Test Case	1- Single Lead	2- 5 Leads
T surrounding	50 deg C	50 deg C
Current/Lead	0.33 Amp	0.33 Amp
Estimated Lead Temperature	59 deg C	76 deg C

Discussions:

1. Temperatures were measured at other locations that were placed gradually away from the powered leads. Based upon those results, it was clear that the polyimide will not provide efficient thermal spreading if a lot of powered leads will be concentrated together.
2. There was a significant lead temperature difference (17 deg C) between a single lead powered on case and 5 leads powered on case. There are two corner sections in the latest Eu TAB frame layout that in each have 32 power leads congregated together right next to each other. This might be a potential thermal problem.
3. I performed the test applying a range of current through the leads. If anyone is interested in that data please let me know.

Please let me know if you guys need clarification on my test setup and assumptions.

Herman

.

From: Richard Dickson [dickson@gamorra]
Sent: Thursday, September 22, 1994 3:43 PM
To: 'euterpe@gamorra'
Subject: csyn error

you'all

here another one i'm not sure of ...

error (DiffInputNodePairCheck.755) in file "tbr_euterpe-pass1.spivs": leaf-inp
ut differential is missing a complementary leaf-input

instance path: top.xxlug_ctrltag_q_9ag_q_9a_42_106p7p_1.xlrsltr9_42
cellname path: top.scsmf3rv3 .is3_ad1ph

instance path: top.xxlug_ctrltag_q_9ag_q_9a_62_126p9p_1.xlrsltr9_n_62
cellname path: top.scsmf3v3 .sis1_ad1ph

dickson

.

From: tbr
Sent: Thursday, September 22, 1994 3:58 PM
To: 'Richard Dickson'
Cc: 'euterpe@gamorra'; 'bill'
Subject: csyn error
Follow Up Flag: Follow up
Flag Status: Red

Richard Dickson wrote (on Thu Sep 22):

you'all

here another one i'm not sure of ...

error (DiffInputNodePairCheck.755) in file "tbr_euterpe-pass1.splvs": leaf-inp
ut differential is missing a complementary leaf-input

instance path: top.xxlug_ctrldatag_q_9ag_q_9a_42_106p7p_1.xlrsltr9_42
cellname path: top.scsmf3rv3.is3_ad1ph

instance path: top.xxlug_ctrldatag_q_9ag_q_9a_62_126p9p_1.xlrsltr9_n_62
cellname path: top.scsmf3v3.sis1_ad1ph

I think bill may need to look at the 3rd stage XLU schematic to track
this one down.

Tim

From: Tim B. Robinson [tbr@aphrodite]
Sent: Thursday, September 22, 1994 3:58 PM
To: 'Richard Dickson'
Cc: 'euterpe@gamorra'; 'bill@aphrodite'
Subject: csyn error

Richard Dickson wrote (on Thu Sep 22):

```
you'all

here another one i'm not sure of ...

error (DiffInputNodePairCheck.755) in file "tbr_euterpe-pass1.splvs":
leaf-inp
  ut differential is missing a complementary leaf-input

      instance path:
top.xxlug_ctrlldatag_q_9ag_q_9a_42_106p7p_1.xlrsltr9_42
      cellname path: top.scsmf3rv3.is3_adlph

      instance path:
top.xxlug_ctrlldatag_q_9ag_q_9a_62_126p9p_1.xlrsltr9_n_62
      cellname path: top.scsmf3rv3
.sis1_adlph
```

I think bill may need to look at the 3rd stage XLU schematic to track this one down.

Tim

.

From: tbr
Sent: Thursday, September 22, 1994 4:07 PM
To: 'Richard Dickson'
Subject: euterpe/verilog/bsrc/es escntrl.V
Follow Up Flag: Follow up
Flag Status: Red

Richard Dickson wrote (on Thu Sep 22):

Update of /p/cvsroot/euterpe/verilog/bsrc/es
In directory rhodan:/N/rama/root/s5/dickson/euterpe/verilog/bsrc/es

Modified Files:
escntrl.V

Log Message:
fix csyn error

How come non of these have shown up in simulation?

Tim

Tim

.

From: Wayne Freitas [wayne@echidna]
Sent: Thursday, September 22, 1994 6:11 PM
To: 'graham@echidna'; 'yves@echidna'
Cc: 'hestia@echidna'
Subject: Meeting minutes from Part 68 review

These are the notes I took, please comment if I've missed anything.

Part 68 preliminary review

Attendee's: Graham, Jean-Yves, Wayne, Cliff Denchfield.

Gave a simple over to Cliff of our product and how the phone interface would be used. Explained that primary use of phone jack was for the unit to dial out for billing or status.

Cliff then gave us a summary of registering for part 68 to the FCC.

Application package was submitted with the following data:

- Application form
- Adequacy agreement form
- Data on phone jack
- Exhibit "D" Description of Unit
 - brochure
 - or write-up on product
- Exhibit "E" Technical Information
 - Block diagram of circuitry pertaining to the phone
 - Parts lists
 - Photo of top and bottom of PCA
- Exhibit "F"
 - Test data these are the test that he performs
 - Signal Power level in/out of band
 - Line balance
 - DTMF
 - Ringer equivalent
 - Environmental temp
 - Hi-pot
 - Surge
- Exhibit "G1" bit bucket
 - Q.A. plan
 - Compliance test plan
 - Label info and location
 - User info (manual)

All this information is open to public records except for Exhibit "E" if you indicate that it is confidential.

During the test process the product is tested for performance, then is ran through the environmental test and back through performance.

Cliff indicated that the tests takes 3 working days and that it typically takes 3 - 5 weeks for the FCC to approve.

We also found out that there are 3 catagories that we can file for.

Dialing, No dialing, and Multimedia. Discussion centered around the difference between Dialing which is typical for your standard modem and Multimedia. It seems that if we registered for Dialing and what to incorporate Fax or Audio at a later date we would have to refile. This would limit us to not being able to upgrade new software features such a fax features into or exsisting products out in the field without putting on a new label. We also discussed that the unit was able to be upgraded remotely (V22.bis, V32, Fax, etc) and how would this affect our filing. Cliff is going to check into if we can apply and also into if we can apply for a Multimedia catagory even if we don't have the feature incorporated at the time of registration.

Cliff gave a brief overview of the difference between Part 68 and Canada's DOC CS03.

We then reviewed the board and parts list and found out that we need to change the surge protection resistors to 10 ohm metal oxide and the EMI caps to support a rating of 1500 VAC for high-pot testing.

The last issue involved the DAA, where do to some tricky labeling we end up being responsible for making sure that the DAA will meet our requirements. The outcome was that we would need to notify Mfg. that a QA incoming inspection and test procedure needed to be put into place.

Action items:

Cliff to review catagory listing to see if we can apply for Multimedia, and if it support soft field upgrades.

Cliff to provide detailed/technical information on tests ran during verification process.

Cliff to provide difference between FCC and DOC

Cliff to provide document of sequence of procedures for getting Hestia through FCC Part 68.

Wayne to find vendor contact name for RJ11 jack so Cliff can submit request for Manufacurers compliance to Part 68 requirements.

From: Tom Karzes [karzes@microunity.com]
Sent: Thursday, September 22, 1994 7:36 PM
To: 'sofheads@microunity.com'; 'euterpe@microunity.com'
Subject: field deposit/withdraw immediate assignments

Hi folks,

I just want to make yet another correction to what I said at the software meeting today. It turns out that the immediate assignments for the field deposit/withdraw instructions were reversed in the encoding table, not the instruction descriptions. The hardware, software, tests, and documentation are being changed to reflect this.

So, if you have an old copy of the documentation, you need to change the column names of the encoding table to correspond to what's shown below.

Guillermo is changing the assembler and simulator to reflect these changes. However, I believe he plans to keep the assembler syntax as it currently is, so be warned.

The correct immediate assignments for field deposit/withdraw are:

```
use (imm1 & (size - 1)) as shift amount
use (imm2 & (size - 1)) as fsize - 1
```

Encoding Table:

size	amount	fsize - 1	imm1	imm2
64	abcdef	pqrstu	abcdef	pqrstu
32	0bcdef	0qrstu	1bcdef	1qrstu
16	00cdef	00rstu	11cdef	11rstu
8	000def	000stu	111def	111stu
4	0000ef	0000tu	1111ef	1111tu
2	00000f	00000u	11111f	11111u
1	000000	000000	111111	111111

Range restriction:

```
0 <= amount < size
1 <= fsize <= size - amount
```

The group size can be obtained from imm1 & imm2 as follows:

imm1 & imm2	size
0xxxxx	64
10xxxx	32
110xxx	16
1110xx	8
11110x	4
111110	2
111111	1

Illegal combinations occur when $\text{imm1} + \text{imm2} \geq \text{size}$, in which case an exception should be generated.

Tom Karzes

.

From: Ken Hsieh [ken@clytemnestra]
Sent: Thursday, September 22, 1994 7:46 PM
To: 'tbr@aphrodite'
Subject: Ticket 492: godzilla / full

tbr wrote:

```
>  
> Root file system on godzilla is full.  
>  
> tbr@godzilla ~/euterpe/verilog/bsrc/hc 493 % df /  
> Filesystem      kbytes  used  avail capacity Mounted on  
> /dev/sd0a        15671  14996    0 106% /  
> tbr@godzilla ~/euterpe/verilog/bsrc/hc 494 %  
> /: write failed, file system is full  
>  
> /: write failed, file system is full
```

Cleaned.

ken

From: Tim B. Robinson [tbr@aphrodite]
Sent: Thursday, September 22, 1994 8:00 PM
To: 'graham@aphrodite'; 'tbe@aphrodite'; 'ras@aphrodite'; 'yves@aphrodite'; 'rich@aphrodite'; 'bfox@aphrodite'
Cc: 'hestia@aphrodite'; 'pmayer@aphrodite'
Subject: Main board placement

We have enough placement done on the main board to know where the major problems are. I'd like to meet in the morning at 10am (eng conference room) to decide how to proceed. Copies of the plot have been distributed.

Major areas of concern are:

1. via fannout around calliope/euterpe. Current design rules seem to indicate we have to go a considerable distance before having enough room to drop vias. This is bad for the decoupling caps for two reasons. First we get longer than desirable traces; second the via field then takes up most of the room leaving not enough space to fit in all the caps.
2. It's marginal as to whether there is sufficient area in the cable section to accommodate all the components.
3. There is no room to fit the contingency VCOs.
4. Some of the baluns have been pushed out into the digital area. There is in fact no way to get the required traces to them with the current keep outs, but in addition this location is not acceptable for noise reasons.

There is good news! We appear to have no problems in the digital area, or with the audio, video, and phone sections.

Tim

.

From: tbr
Sent: Thursday, September 22, 1994 8:30 PM
To: 'trouble@clytemnestra'
Subject: Ticket 492: godzilla / full
Follow Up Flag: Follow up
Flag Status: Red

Ken Hsieh wrote (on Thu Sep 22):

tbr wrote:

```
>  
> Root file system on godzilla is full.  
>  
> tbr@godzilla ~/euterpe/verilog/bsrc/hc 493 % df /  
> Filesystem      kbytes  used  avail capacity Mounted on  
> /dev/sd0a        15671  14996    0 106% /  
> tbr@godzilla ~/euterpe/verilog/bsrc/hc 494 %  
> /: write failed, file system is full  
>  
> /: write failed, file system is full
```

Cleaned.

Thanks

Tim

From: lisa
Sent: Thursday, September 22, 1994 8:42 PM
To: 'software-checkins-dist'
Subject: gnu-tools/sim/terp memory.h memory.c execloop.c

Update of /p/cvsroot/gnu-tools/sim/terp
In directory calliope:/N/hyperion/root/s1/lisa/gnu-tools/sim/terp

Modified Files:
memory.h memory.c execloop.c

Log Message:

Yet another hack for endianness problems -- now even the easy cases in execute_loop must call move_data (which had to be exported from memory.c so that it could be called). Of course, if we are willing to do this, we could just as well do the hard cases here, too. Better would be to rework this stuff so that it's both organized and optimized (and correct :-).

.

From: tbe@MicroUnity.com
Sent: Thursday, September 22, 1994 10:05 PM
To: 'Patricia Mayer'
Cc: 'tbr'; 'bfox'; 'jt'
Subject: Re: main PCB questions

>Hi Tom!
>
>I've had several questions come up since you've been gone...Heres my list:
>
>* Is my SD RAM Placement OK?

Looks good to me as long as the vias are outside of the primary and secondary side keep-outs.

>
>* Where does the Smart card connector go?
>

I can go with either between the SDRAMs and the big fan hole in the middle of the pcb, or "above" the fan hole in the RF section (doesn't strike me as too good from a noise standpoint here though). What does the rat's nest indicate? I can't tell which component that connector is from the plot, so I'll stop by first thing Friday morning to find out.

>* Am I working with the actual dimensions of the board outline or is this the >"box" outline? What is the actual X,Y of Caliope and Euterpe?
>

Absolutely the pcb outline, the x and y of Calliope and Euterpe is per the dimensions on sheet 1 of the dxf. However, these dimensions will have to be translated to the tooling holes which are not place yet, where we will strike the pcb's datums.

>* I understand there is a hole under Caliope and Euterpe, can I route under >the chip and around that hole?
>

There is no hole under Calliope or Euterpe--someone's spreading rumors. There are keepouts on the secondary side for the "X" shaped chip retainer, and primary side partial ground planes under Calliope and Euterpe (thought these should be defined by the prt file just like the TAB OLB pads, but I never checked this). These planes should be slightly larger than the space transformers of those two chips, both of which will constrain the ability to route under the chip/TAB. Sorry if they were missed--they're definitely needed as they are the only path for the DC ground from the chips to the pcb.

>* Which is which, on the three F connectors?
>

Sorry I didn't define this with Brian. I think my external design considerations should be secondary to pcb placement and hookup requirements, so I've cc'd him to get his input (if he hasn't provided it already).

>* The Via fan-out we discussed isn't going to work... minimum spacing is
>really
>trace to trace with NO room for vias. Talked to John about this and he had a
>suggestion that I'd like to talk to you about. I have the new via area drawing.
>

I'll come by asap Friday.

 \succ

>Any other ideas or news? - Pattie

I will have a revised criteria drawing that will fill in remaining blanks (let's go over them tomorrow) and incorporate the items discussed above by Monday.

-Tom

Tom Eich tbe@microunity.com
MicroUnity Systems Engineering, Inc.
255 Caspian Dr. Sunnyvale, CA 94089
(408)734-8100, (408)734-8136 fax

From: Mark Hofmann [hopper@boreas]
Sent: Thursday, September 22, 1994 10:15 PM
To: 'Geert Rosseel'
Subject: Re: ctio

Geert Rosseel writes:

I noticed a ctiod and ctioi in ~chip/euterpe/verilog/bsrc/ctio ..
Did you change that to 0/1 already in the Makefiles ? If so, Can you/I realese
it to get ythese versions. You
should do a claen first to get rid of the *d and *i
files

Aaargh! I _fixed_ this. Anyway, I fixed it again. It's building now.
Sorry.

-mark

.

From: tbe@MicroUnity.com
Sent: Thursday, September 22, 1994 10:31 PM
To: 'Tim B. Robinson'
Cc: 'pmayer@MicroUnity.com'; 'hestia@MicroUnity.com'; 'graham@MicroUnity.com';
'ras@MicroUnity.com'; 'yves@MicroUnity.com'; 'rich@MicroUnity.com'; 'bfox@MicroUnity.com'
Subject: Re: Main board placement

tbr wrote:

>We have enough placement done on the main board to know where the
>major problems are. I'd like to meet in the morning at 10am (eng
>conference room) to decide how to proceed. Copies of the plot have
>been distributed.

>
>Major areas of concern are:

>
>1. via fannout around calliope/euterpe. Current design rules seem to
>indicate we have to go a considerable distance before having enough
>room to drop vias. This is bad for the decoupling caps for two
>reasons. First we get longer than desirable traces; second the via
>field then takes up most of the room leaving not enough space to fit
>in all the caps.

>
>2. It's marginal as to whether there is sufficient area in the cable
>section to accommodate all the components.

>
>3. There is no room to fit the contingency VCOs.

>
>4. Some of the baluns have been pushed out into the digital area.
>There is in fact no way to get the required traces to them with the
>current keep outs, but in addition this location is not acceptable for
>noise reasons.

>

I think the keep outs you refer to above are just my first stab at supreme
isolation, and were made to be changed. I'll be there at 10:00am.

>There is good news! We appear to have no problems in the digital
>area, or with the audio, video, and phone sections.

>
>Tim

Hooray!

-Tom

Tom Eich tbe@microunity.com
MicroUnity Systems Engineering, Inc.
255 Caspian Dr. Sunnyvale, CA 94089
(408)734-8100, (408)734-8136 fax

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From: Geert Rossee! [geert@ambiorix]
Sent: Thursday, September 22, 1994 10:49 PM
To: 'tbr@ambiorix'
Subject: vfiles in rg

Hi Tim,

There is nor vfiles file in /u/chip/euterpe/verilog/bsrc/rg

Geert

.

From: Geert Rosseel [geert@ambiorix]
Sent: Thursday, September 22, 1994 11:07 PM
To: 'tbr@ambiorix'
Subject: help on toplevel build

Hi Tim,

I cannot get passed the v2e step . The output is
in ~geert/chip/euterpe/verilog/bsrc/geert_v2e.log

Can you have a look at it.

My xterm is not working propoerly so I am not
sure hoe much I can get done today.

Geret

.

From: Jay Tomlinson [woody@demeter]
Sent: Thursday, September 22, 1994 11:52 PM
To: 'euterpe@demeter'
Subject: IMMINENT Decision: Data Cache Tag bits 63:48 ignored by hardware.

Decision to become final at midnight on Monday 9/26/94.

The data cache tag currently consists of:

63:6 physical address of the data.
5:1 protection information
0 dirty bit.

the physical address is compared to the physical address generated by the instruction. If they match then the cache data can be used. If they do not match, then the physical address (generated by the instruction) will be used to fetch the data to be written into the cache.

Also, if physical address bits 63:48 are not all zero, then an Illegal Address exception will be reported and the cache data will not be fetched and written into the data cache. This means that the hardware will never write the tag with any of bits 63:48 non-zero as part of a cache fill. The only way that any of these bits can be written non-zero, is by SW (store directly to the data cache tag). If SW does this, then when the cache line is accessed either a cache miss will occur or an exception will be reported due to the physical address having non-zero a value in bits 63:48.

This means that bits 63:48 are essentially useless since they can never be non-zero and meaningful.

Therefore I propose that the cache tag be logically viewed as only consisting of bits 47:6 of the physical address. These bits would not be matched to the physical address and would written/read as zero.

Jay

.

From: tbr
Sent: Friday, September 23, 1994 12:40 AM
To: 'Geert Rosseel'
Subject: vfiles in rg
Follow Up Flag: Follow up
Flag Status: Red

Geert Rosseel wrote (on Thu Sep 22):

Hi Tim,

There is nor vfiles file in /u/chip/euterpe/verilog/bsrc/rg

Strange. I must have missed deleting an old v2e rule from the makefile. I'll take a look.

Tim

From: Tim B. Robinson [tbr@aphrodite]
Sent: Friday, September 23, 1994 12:40 AM
To: 'Geert Rosseel'
Subject: vfiles in rg

Geert Rosseel wrote (on Thu Sep 22):

Hi Tim,

There is nor vfiles file in /u/chip/euterpe/verilog/bsrc/rg

Strange. I must have missed deleting an old v2e rule from the makefile. I'll take a look.

Tim

.

From: tbr
Sent: Friday, September 23, 1994 12:43 AM
To: 'Geert Rosseel'
Subject: vfiles in rg
Follow Up Flag: Follow up
Flag Status: Red

Geert Rosseel wrote (on Thu Sep 22):

Hi Tim,

There is nor vfiles file in /u/chip/euterpe/verilog/bsrc/rg

I see why. There is a hack, because we currently have rgxmit in the same directory and I had to do some foolery to exclude those files.

I have gone in as chip and made vfiles by hand. If I can get a BOM at the top level for lisar, I'll then look at splitting out rgxmit into a separate directory. This will then fix the problem.

Tim

From: Tim B. Robinson [tbr@aphrodite]
Sent: Friday, September 23, 1994 12:44 AM
To: 'Geert Rosseel'
Subject: vfiles in rg

Geert Rosseel wrote (on Thu Sep 22):

Hi Tim,

There is nor vfiles file in /u/chip/euterpe/verilog/bsrc/rg

I see why. There is a hcak, because we currently have rgxmit in the same directory and I had to do some foolery to exclude those files.

I have gone in as chip and made vfiles by hand. If I can get a BOM at the top level for lisar, I'll then look at splitting out rgxmit into a separate directory. This will then fix the problem.

Tim

.

From: tbr
Sent: Friday, September 23, 1994 12:46 AM
To: 'Geert Rosseel'
Subject: help on toplevel build
Follow Up Flag: Follow up
Flag Status: Red

Geert Rosseel wrote (on Thu Sep 22):

Hi Tim,

I cannot get passed the v2e step . The output is
in ~geert/chip/euterpe/verilog/bsrc/geert_v2e.log

Can you have a look at it.

My xterm is not working propoerly so I am not
sure hoe much I can get done today.

I'll take a look.

Tim

From: Tim B. Robinson [tbr@aphrodite]
Sent: Friday, September 23, 1994 12:46 AM
To: 'Geert Rosseel'
Subject: help on toplevel build

Geert Rosseel wrote (on Thu Sep 22):

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Can you have a look at it.

My xterm is not working propoerly so I am not
sure hoe much I can get done today.

I'll take a look.

Tim

.

From: tbr
Sent: Friday, September 23, 1994 12:47 AM
To: 'Geert Rosseel'
Subject: help on toplevel build
Follow Up Flag: Follow up
Flag Status: Red

Geert Rosseel wrote (on Thu Sep 22):

Hi Tim,

I cannot get passed the v2e step . The output is
in ~geert/chip/euterpe/verilog/bsrc/geert_v2e.log

Can't find this file. Is there a typo?

Tim

From: Tim B. Robinson [tbr@aphrodite]
Sent: Friday, September 23, 1994 12:47 AM
To: 'Geert Rosseel'
Subject: help on toplevel build

Geert Rosseel wrote (on Thu Sep 22):

Hi Tim,

I cannot get passed the v2e step . The output is
in ~geert/chip/euterpe/verilog/bsrc/geert_v2e.log

Can't find this file. Is there a typo?

Tim

.

From: tbr
Sent: Friday, September 23, 1994 12:53 AM
To: 'Geert Rosseel'
Subject: help on toplevel build
Follow Up Flag: Follow up
Flag Status: Red

Geert Rosseel wrote (on Thu Sep 22):

Hi Tim,

I cannot get passed the v2e step . The output is
in ~geert/chip/euterpe/verilog/bsrc/geert_v2e.log

Can you have a look at it.

Found it. It's getting the wrong v2e rule from somewhere, but I
haven't figured out where yet . . .

Tim

From: Tim B. Robinson [tbr@aphrodite]
Sent: Friday, September 23, 1994 12:53 AM
To: 'Geert Rosseel'
Subject: help on toplevel build

Geert Rosseel wrote (on Thu Sep 22):

Hi Tim,

I cannot get passed the v2e step . The output is
in -geert/chip/euterpe/verilog/bsrc/geert_v2e.log

Can you have a look at it.

Found it. It's getting the wrong v2e rule from somewhere, but I haven't figured out where
yet . . .

Tim

.

From: tbr
Sent: Friday, September 23, 1994 1:20 AM
To: 'Geert Rosseel'
Subject: help on toplevel build
Follow Up Flag: Follow up
Flag Status: Red

Geert Rosseel wrote (on Thu Sep 22):

Hi Tim,

I cannot get passed the v2e step . The output is
in ~geert/chip/euterpe/verilog/bsrc/geert_v2e.log

Can you have a look at it.

Well, it took a while to figure it out, but here's what happened.

The rule in Makefile for \$(GARDS_DIR)/%_euterpe.v2e depends on vfiles (even though it does not actually use vfiles to figure out what files to link - it can't because you may not want all of them depending what you exclude). However, your vfiles is not up to date. Now er have the old generic rule in Makefile.rules, and gmake is deciding to use that one. It's stupid the way it chooses (thought the documentation is clear). If there are two matching rules the first one is chosen *unless* that rule would require a dependency to be remade whereas the second one would not. (It's a useless definition because which rule you get depends on just what files are lying round - it would be much more sensible for it to pick the first matching rule even if it did need to make a dependency.)

I have not bumped into this before because I have been in the habit of doing a make updatedirs before trying a top level run to be sure all my sub dirs are built. That of course leaves an up to date vfiles. I just tried it now without makin updatedirs and sure enough it fails the same way.

I'm pretty sure the old generic rule is not used anywhere so I'm going to comment it out. I'll release a new Makefile.rules.

Tim

From: Tim B. Robinson [tbr@aphrodite]
Sent: Friday, September 23, 1994 1:20 AM
To: 'Geert Rosseel'
Subject: help on toplevel build

Geert Rosseel wrote (on Thu Sep 22):

Hi Tim,

I cannot get passed the v2e step . The output is
in ~geert/chip/euterpe/verilog/bsrc/geert_v2e.log

Can you have a look at it.

Well, it took a while to figure it out, but here's what happened.

The rule in Makefile for \$(GARDS_DIR)/%_euterpe.v2e depends on vfiles (even though it does not actually use vfiles to figure out what files to link - it can't because you may not want all of them depending what you exclude). However, your vfiles is not up to date. Now er have the old generic rule in Makefile.rules, and gmake is deciding to use that one. It's stupid the way it chooses (thought the documentation is clear). If there are two matching rules the first on is choses *unless* that roul would require a dependency to be remade wheras the second one would not. (It's a useless definition because which rule you get depends on just what files are lying round - it would be much more sensible for it to pick the first matching rule even if it did need to make a dependency.)

I have not bumped into this before because I have been in the habit of doing a make updatedirs before trying a top level run to be sure all my sub dirs are built. That of course leaves an up to date vfiles. I just tried it now without makin updatedirs and sure enough it fails the same way.

I'm pretty sure the old generic rule is not used anywhere so I'm going to comment it out. I'll release a new Makefile.rules.

Tim

.

From: tbr
Sent: Friday, September 23, 1994 2:18 AM
To: 'doi'
Subject: releasebom
Follow Up Flag: Follow up
Flag Status: Red

I needed to do a releasebom in euterpe/verilog/bsrc. I deliberately wanted a downrev BOM in a sub directory (because the latest BOM in that sub-dir has introduced a problem). I got an error, because that BOM also added a file, which of course I do not have in the downrev BOM:

Releasing BOM in /n/auspex/s15/tbr/euterpe/verilog/bsrc/cc
mkbom: The following is found in the repository (and the most recent BOM), but not locally:
mkbom:
mkbom: Files : .checkoutrc
mkbom:
mkbom: Error: Local directory is out-of-date with respect to the repository.
Problems with mkbom - return code 1

I thought I was supposed to be a bel to release a BOM even though my local copy is down rev just as long as I have nothing uncommitted?

Tim

.

From: tbr
Sent: Friday, September 23, 1994 2:47 AM
To: 'doi'
Subject: releasebom
Follow Up Flag: Follow up
Flag Status: Red

OK, so I backed out cc, by doing:

```
getbom -r 9.0
mv BOM foo
cvs update BOM
mv foo BOM
cvs ci -m 'something about backing out' BOM
```

Then I tried to release at the top again and it still failed the same way.

Now, cvs status BOM seems to tell me 10.0 is the latest and my check in does not show up at all:

```
tbr@rhodan ~/euterpe/verilog/bsrc/cc 424 % cvs log BOM | more
```

```
RCS file: /u/chip/chip-archive/euterpe/verilog/bsrc/cc/BOM,v
Working file: BOM
head: 10.0
branch:
locks: strict
access list:
symbolic names:
comment leader: "# "
keyword substitution: kv
total revisions: 18;   selected revisions: 18
description:
releasebom adding BOM
```

```
-----
revision 10.0
date: 1994/09/20 20:18:17 LT; author: geert; state: Exp; lines: +1 -1
Release Target: euterpe/verilog/bsrc/cc
```

Run cc in /u/chip

Yet if I look in my CVS/Entries file, the .checkoutrc (which was the file added in 10.0) is no longer there (ie it was removed by the getbom -r 9.0).

```
tbr@rhodan ~/euterpe/verilog/bsrc/cc 425 % more CVS/Entries
/cctester.h/1.1/Fri Jul 8 11:18:36 1994 Thu Jun 30 16:23:27 1994//
/cccounter.pla/1.3/Mon Aug 15 21:13:49 1994 Mon Aug 15 21:13:49 1994//
/ccinprog.pla/1.2/Mon Aug 15 21:13:50 1994 Mon Aug 15 21:13:50 1994//
/ccdecode.pla/1.3/Tue Sep 13 20:06:09 1994 Tue Sep 13 20:06:08 1994//
/power.tab.local/5.1/Tue Sep 13 20:06:14 1994 Thu Sep 8 16:29:43 1994//
```

/Makefile/1.5/Thu Sep 22 23:40:40 1994 Thu Sep 22 23:40:40 1994//
/cc.V/1.9/Thu Sep 22 23:40:42 1994 Thu Sep 22 23:40:41 1994//
/cc.ut/1.2/Thu Sep 22 23:40:43 1994 Thu Sep 22 23:40:43 1994//
/cc_control.pim/5.6/Thu Sep 22 23:40:45 1994 Thu Sep 22 23:40:45 1994//
/ccnbgo.Veqn/4.1/Thu Sep 22 23:40:47 1994 Thu Sep 22 23:40:47 1994//
/cctester.V/1.3/Thu Sep 22 23:40:49 1994 Thu Sep 22 23:40:49 1994//
/genpim.pl/5.3/Thu Sep 22 23:40:51 1994 Thu Sep 22 23:40:51 1994//
/pimlib.pl/5.2/Thu Sep 22 23:40:53 1994 Thu Sep 22 23:40:53 1994//
/BOM/10.0/Fri Sep 23 00:22:42 1994 Fri Sep 23 00:13:07 1994//

Which shows the V 10.0 BOM, but the other files listed are from the 9.0 BOM.

Baffled. Lisar is trying to do it now 'cause she doesn't believe me .

..

Tim

.

From: Derek Iverson [doi@demeter]
Sent: Friday, September 23, 1994 10:37 AM
To: 'Tim B. Robinson'
Subject: releasebom

Tim B. Robinson writes:

> Releasing BOM in /n/auspex/s15/tbr/euterpe/verilog/bsrc/cc
> mkbom: The following is found in the repository (and the most recent BOM), but not locally:
> mkbom:
> mkbom: Files : .checkoutrc
> mkbom:
> mkbom: Error: Local directory is out-of-date with respect to the repository.
> Problems with mkbom - return code 1
>
>
> I thought I was supposed to be a bel to release a BOM even though my
> local copy is down rev just as long as I have nothing uncommitted?

You can release a BOM even though a local copy is down rev. You can even release a BOM if there are files or directories in the repository that you do not have checked out *IF* they are not included in the most recent BOM. The problem you are having is that the .checkoutrc file is already part of the most recent BOM so you must also have it.

doi

.

From: Lisa Robinson [lisar@rhodan]
Sent: Friday, September 23, 1994 1:05 PM
To: 'sysadm@rhodan'
Cc: 'tbr@rhodan'
Subject: aphrodite

Has 2 processes stuck in DW, could we schedule a reboot after lunch.

lisar 315 0.0 0.181896 152 p0 D Sep 21 1:38 /a/zycad.5.1a/XPLUS5.1a/bin/srl2mm -S ./xp_dir/big_a_euterpe_wrap

lisar 26035 0.0 0.185888 68 p1 D Sep 21 7:02 /n/aphrodite/s3/euterpe/tools/vendor/vxi/vxi_1.1/exe/vxi

Thanks

Lisa R.

From: tbe@MicroUnity.com
Sent: Friday, September 23, 1994 2:00 PM
To: 'hestia'; 'pmayer'; 'rich'; 'yves'; 'ras'; 'woody'; 'albers'; 'tbr'; 'wayne'; 'bfox'; 'arya'; 'graham'; 'dane'
Subject: 9/23 pcb meeting actions

Following are actions and status resulting from the pcb meeting held 9/23/94:

1) The prt files for Calliope and Euterpe do not include the giant ground pad connecting the space transformer to the pcb.

action: Vijay to determine the size of the pad that ensures that the space transformer's indium is always on this pad and not on the solder mask.

action: Patty to revise prt files to include this pad.

action: Jay to revise gyg files to show connection to ground.

2) Decision taken to keep the Hermes channel on the primary side between Calliope and Euterpe. The expansion channel will need to go through vias to the connector; waiting for the ECO to correct connector.

action: Dan Albers to work with Patty to get ECO implemented correctly.

3) SDRAM and analog placement area trade-offs:

action: Patty to pull SDRAM in as close as possible to Euterpe.
NEWSFLASH: tbr and Patty have rearranged the SDRAM all in a line to open more area above SDRAM for VCOs and analog stuff.

action: Patty to place one VCO in space above SDRAM area;

action: tbe to support mechanical revisions to allow this with new criteria drawing.

4) A/V and phone circuits vs. VCO and RF placement area trade-offs.

action: Patty to pinch A/V and phone down to create area for VCO at top right corner of Calliope. Yves and rich to review.

action: Patty to do best fit placement of RF (cable in) circuit; bfox and Arya to support.

action: Patty to place 1080 MHz source as close to Calliope as possible; bfox to review.

5) No decision taken on possibility of eliminating the second receive channel.

action: Patty and all to work toward fitting current netlist on pcb and achieving acceptable hookup; Patty to overlap primary side through-hole devices with secondary side SMT devices to maximum extent possible within design rules.

Please post follow-ups for any other actions or status.

Tom Eich tbe@microunity.com
MicroUnity Systems Engineering, Inc.
255 Caspian Dr. Sunnyvale, CA 94089
(408)734-8100, (408)734-8136 fax

.

From: tbr
Sent: Friday, September 23, 1994 2:25 PM
To: 'ericm'
Subject: More random behavior
Follow Up Flag: Follow up
Flag Status: Red

Fri Sep 23 19:22:49 GMT 1994
HOME=/n/auspex/s15/tbr/euterpe/tools LM_LICENSE_FILE=/n/auspex/s15/tbr/euterpe/tools/sl/license/license.dat
DISPLAY=192.216.194.200:0.0 SL_TOTAL_DURATION=500
CHIPROOT=/n/auspex/s15/tbr/euterpe /n/auspex/s15/tbr/euterpe/tools/bin/net_select -h 84 -P 2 gards/rg-pass1.dff >
rg.short.nets
/bin/sh: /n/auspex/s15/tbr/euterpe/tools/bin/net_select: not found
make[2]: *** [gars/rg-pass2.sdl] Error 1
make[2]: Leaving directory `/N/auspex/root/s15/tbr/euterpe/verilog/bsrc/rg'
make[1]: *** [rg.short.nets] Error 1
make[1]: Leaving directory `/N/auspex/root/s15/tbr/euterpe/verilog/bsrc/rg'
make: *** [rggars] Error 1
/usr/local/bin/pageme: pager: not found
tbr@gamorra ~/euterpe/verilog/bsrc/rg 655 %

.

From: tbr
Sent: Friday, September 23, 1994 2:37 PM
To: 'Lisa Robinson'
Cc: 'sysadm@rhodan'
Subject: aphrodite
Follow Up Flag: Follow up
Flag Status: Red

Lisa Robinson wrote (on Fri Sep 23):

Has 2 processes stuck in DW, could we schedule a reboot after lunch.

```
lisar  315 0.0 0.181896 152 p0 D   Sep 21  1:38 /a/zycad.5.1a/XPLUS5.1a/bin/srl2mm -  
S ./xp_dir/big_a_euterpe_wrap
```

```
lisar  26035 0.0 0.185888  68 p1 D   Sep 21  7:02 /n/aphrodite/s3/euterpe/tools/vendor/vxi/vxi_1.1/exe/vxi
```

Thanks

Lisa R.

When the machine room is down would be a great time.

Tim

.

From: Tom Laidig [tom@cilo]
Sent: Friday, September 23, 1994 3:34 PM
To: 'Tim B. Robinson'
Cc: 'ericm@MicroUnity.com'; 'sysadmin@MicroUnity.com'; 'tom@MicroUnity.com'
Subject: Re: URGENT Re: disk space

Tim B. Robinson writes:

Tom Laidig wrote (on Fri Sep 23):

```
-> df /u/chip/.  
Filesystem      kbytes  used  avail capacity Mounted on  
auspex3:/s10    1240589 1111449  5081  100%  /N/auspex/root/s10  
->
```

This is growing fast, kids. At this rate, we'll be full before the auspex goes down this afternoon.

Can we find a disk QUICKLY to move some stuff to? As mentioned above, I suggest we move /n/auspex/s10/tools (which is /a/muse) somewhere. That'll free up 123Meg.

Looks like there's more I need to push down. We are getting 5-15MB per section, and we have about 25 sections to do. So reconn 200MB more to come if we don't change anything.

Hmm... I found out where a big slug of space went. Sometime yesterday the directory /u/chip/euterpe/verilog/bsrc grew from 29Meg to 56Meg.

--

Tom L

.

From: Tom Laidig [tom@clio]
Sent: Friday, September 23, 1994 3:43 PM
To: 'Tom Laidig'
Cc: 'tbr@aphrodite'; 'ericm@MicroUnity.com'; 'sysadmin@MicroUnity.com'; 'tom@MicroUnity.com'
Subject: Re: URGENT Re: disk space

Tom Laidig writes:

|
| Tim B. Robinson writes:

||
|| Looks like there's more I need to push down. We are getting 5-15MB
|| per section, and we have about 25 sections to do. So recon 200MB
|| more to come if we don't change anything.

|
| Hmm... I found out where a big slug of space went. Sometime yesterday
| the directory /u/chip/euterpe/verilog/bsrc grew from 29Meg to 56Meg.

Sorry, that was a pretty content-free statement. I was emailing while
talking to someone in the office at the same time -- a bad idea.

It turns out that all I _do_ know is that the euterpe/verilog/bsrc/mst
directory grew to 12Meg from some amount that was less than 10Meg; no
other subdirectory of euterpe/verilog/bsrc was or is bigger than
10Meg.

--
Tom L

.

From: tbr
Sent: Friday, September 23, 1994 3:44 PM
To: 'tom'
Cc: 'ericm'
Subject: /s37
Follow Up Flag: Follow up
Flag Status: Red

I just took a look how we are doing there, and that's alarming too:

```
tbr@staypuft ~/euterpe/verilog/bsrc 684 % df /n/auspex/s37
Filesystem      kbytes  used  avail capacity  Mounted on
auspex0:/s37    1847292 967855 787072   55%    /N/auspex/root/s37
```

This will easily grow a few hundred MB more over the weekend.

Assuming we have another partition available, it's trivial to move some symlinks to stop it eventually overflowing.

Tim

.

From: tbr
Sent: Friday, September 23, 1994 3:45 PM
To: 'Tom Laidig'
Cc: 'ericm@MicroUnity.com'; 'sysadmin@MicroUnity.com'; 'tom@MicroUnity.com'
Subject: Re: URGENT Re: disk space
Follow Up Flag: Follow up
Flag Status: Red

Tom Laidig wrote (on Fri Sep 23):

Tim B. Robinson writes:

Tom Laidig wrote (on Fri Sep 23):

```
-> df /u/chip/.
Filesystem      kbytes  used  avail capacity Mounted on
auspex3:/s10    1240589 1111449  5081  100%  /N/auspex/root/s10
->
```

This is growing fast, kids. At this rate, we'll be full before the auspex goes down this afternoon.

Can we find a disk QUICKLY to move some stuff to? As mentioned above, I suggest we move /n/auspex/s10/tools (which is /a/muse) somewhere. That'll free up 123Meg.

Looks like there's more I need to push down. We are getting 5-15MB per section, and we have about 25 sections to do. So recon 200MB more to come if we don't change anything.

Hmm... I found out where a big slug of space went. Sometime yesterday the directory /u/chip/euterge/verilog/bsrc grew from 29Meg to 56Meg.

Yep, mostly in the mst directory. I expect es, mc, gf to grow over the weekend too. I'll do another round of Makefile surgery at the weekend to alleviate some of this.

Tim

From: Kevin Peterson [khp@MicroUnity.com]
Sent: Friday, September 23, 1994 5:42 PM
To: 'abbott@MicroUnity.com'
Subject: QAM/"terp track" receiver schedule

Here's what I've got in my working schedule... what do you think?

tasks done	expect	accum
---------------	--------	-------

Terp track		
1.0 cable-in rewrite/cleanups	1w	1w
decision directed carrier recovery	8d	3d
* integrate blind timing recovery	2d	
integrate lms eq update	5d	
fix symbol mapping (w differential) (brendan)		5d
integrate blind eq update	8d	
* integrate blind carrier recovery	3d	
fix gain adjust	1d	
implement receiver reset	1d	
tune error metrics and state transitions	1w	
channel changing/reacquisition	2w	

* waiting on henry

-Kevin

.

From: tbr
Sent: Saturday, September 24, 1994 2:24 PM
To: 'Mark Hofmann'
Subject: euterpe/verilog/bsrc/ck cktop.V
Follow Up Flag: Follow up
Flag Status: Red

Mark Hofmann wrote (on Sat Sep 24):

Update of /p/cvsroot/euterpe/verilog/bsrc/ck
In directory cyclops:/N/auspex/root/s32/hopper/chip/euterpe/verilog/bsrc/ck

Modified Files:
cktop.V

Log Message:
removed fgen.

Have you updated the top level to be consistent with this?

Tim

.

From: Lisa Robinson [lisar@nosferatu]
Sent: Saturday, September 24, 1994 2:47 PM
To: 'dickson@nosferatu'
Cc: 'veena@nosferatu'; 'tbr@nosferatu'
Subject: datapath

Rich I have been running the datapath tests - ones that have run ok in the past - and many fail.

I have rebuilt the tests recently but they tests do run on terp.

I am just about to get a dump of eor for you but here is some of list.

```
dpeandispc Creating dpeandispc.dpo .... Ran ok
dpeandnspc Creating dpeandnspc.dpo .... (looks like X's) Failed
dpeandspc Creating dpeandspc.dpo .... (looks like X's) Failed
dpenandispc Creating dpenandispc.dpo .... Ran ok
dpenandspc Creating dpenandspc.dpo .... (looks like X's) Failed
dpeesumspc Creating dpeesumspc.dpo .... (looks like X's) Failed
dpemuxspc Creating dpemuxspc.dpo .... Ran ok
dpenorispc Creating dpenorispc.dpo .... Ran ok
dpenorspc Creating dpenorspc.dpo .... (looks like X's) Failed
dpeorispc Creating dpeorispc.dpo .... Ran ok
dpeornspc Creating dpeornspc.dpo .... (looks like X's) Failed
dpeorspc Creating dpeorspc.dpo .... (looks like X's) Failed
dpexnorspc Creating dpexnorspc.dpo .... (looks like X's) Failed
dpexorispc Creating dpexorispc.dpo .... Ran ok
dpexorspc Creating dpexorspc.dpo .... (looks like X's) Failed
```

and many of the set's too.

Lisa R.

From: vant [vanthof@hestia]
Sent: Saturday, September 24, 1994 4:10 PM
To: 'Tom Vo'; 'B. P. Wong'; 'Eldred Fellas'
Cc: 'Dave Van't Hof'; 'Mark Hofmann'; 'Geert Rosseel'; 'Lisa Robinson'; 'Tim B. Robinson'
Subject: gtlb drc'

Tom,
The gtlb drc run finished this morning. I started one up after the machine room came back up. There are 4 poly spacing errors and since I can't look at it from home, I don't know how severe it is. I expect these to be boundary errors only.

If you want to start using the gtlb, I think it would be safe to do so.

Eldred, if you want to see the errors, the error file is:

/u/vanthof/compass/mobi/euterpe/gtlb.err

Thanks,
Dave

--
Dave Van't Hof vanthof@microunity.com MicroUnity Systems Engineering,
Inc.
"What rolls down stairs, alone or in pairs, rolls over the neighbor's dog?"

What's great for a snack and fits on your back? It's log, log, log!"
LOG from BLAMMO! (tm) All kids love Log! #include
<std_disclaim.h>

.

From: tbr
Sent: Saturday, September 24, 1994 5:27 PM
To: 'ericm'
Cc: 'gmo'; 'brendan'; 'geert'; 'hopper'
Subject: NFS time warp
Follow Up Flag: Follow up
Flag Status: Red

I have been trying to track down why it is our big Makefiles apparanly at random sometimes seem to remake things unnecessarily. This has become an increasingly serious problem as some of the unnecessary steps that get triggered often take hours to re-run.

I witnessed a particularly simple, reproducible case and the problem seems to be related to the dates on files in different file systems connected by symlinks.

In this case I have a directory under my home directory on the auspex, which contains a symlink to a local file system on gamorra. I was working on gamorra. Make first created a file in the upper directory, then ran a rule which depended on that file to make another file which is dropped into the lower directory (via the symlink). The problem is that this second file seems to end up with a date before that of the first created file.

Subsequently, another make thinks it has to run this step again. When this is at the front of a long chain of rules, large amounts of work get done over.

I ran the following:

```
tbr@gamorra ~/euterpe/verilog/bsrc/cdio 473 % rsh auspex date ; date ; touch foo ; touch gards/foo ; ls -ls foo gards/foo
Sat Sep 24 15:19:17 PDT 1994
Sat Sep 24 15:18:27 PDT 1994
 0 -rw-rw-r-- 1 tbr      0 Sep 24 15:19 foo
 0 -rw-rw-r-- 1 tbr      0 Sep 24 15:18 gards/foo
```

and indeed the date on gamorra is behind the date on the auspex and furthermore the files now look to have been created in the opposite order from what they really were.

How accurately is time supposed to be synced up between the machines? Given the sizes of the files we are having to handle, symlinks are necessary (I have over 2GB linked this way in my euterpe tree onto local disks on gamorra and staypuft). If dates can only be guaranteed to a certain accuracy, we may have to insert sleep commands into the Makefile to try and deal with this.

Tim

From: Tim B. Robinson [tbr@aphrodite]
Sent: Saturday, September 24, 1994 5:27 PM
To: 'ericm@aphrodite'
Cc: 'gmo@aphrodite'; 'brendan@aphrodite'; 'geert@aphrodite'; 'hopper@aphrodite'
Subject: NFS time warp

I have been trying to track down why it is our big Makefiles apparantly at random sometimes seem to remake things unnecessarily. This has become an increasingly serious problem as some of the unnecessary steps that get triggered often take hours to re-run.

I witnessed a particularly simple, reproducible case and the problem seems to be related to the dates on files in different file systems connected by symlinks.

In this case I have a directory under my home directory on the auspex, which contains a symlink to a local file system on gamorra. I was working on gamorra. Make first created a file in the upper directory, then ran a rule which depended on that file to make another file which is dropped into the lower directory (via the symlink). The problem is that this second file seems to end up with a date before that of the first created file.

Subsequently, another make thinks it has to run this step again. When this is at the front of a long chain of rules, large amounts of work get done over.

I ran the following:

```
tbr@gamorra ~/euterpe/verilog/bsrc/cdio 473 % rsh auspex date ; date ; touch foo ; touch
gards/foo ; ls -ls foo
gards/foo Sat Sep 24 15:19:17 PDT 1994 Sat Sep 24 15:18:27 PDT 1994
  0 -rw-rw-r--  1 tbr          0 Sep 24 15:19 foo
  0 -rw-rw-r--  1 tbr          0 Sep 24 15:18 guards/foo
```

and indeed the date on gamorra is behind the date on the auspex and furthermore the files now look to have been created in the opposite order from what they really were.

How accurately is time supposed to be synced up between the machines? Given the sizes of the files we are having to handle, symlinks are necessary (I have over 2GB linked this way in my euterpe tree onto local disks on gamorra and staypuft). If dates can only be guaranteed to a certain accuracy, we may have to insert sleep commands into the Makefile to try and deal with this.

Tim

From: Tom Vo [vo@merope]
Sent: Saturday, September 24, 1994 9:18 PM
To: 'vant'
Cc: 'vo@hestia'; 'bpw@hestia'; 'efelias@hestia'; 'vanthof@hestia'; 'hopper@hestia'; 'geert@hestia'; 'lisar@hestia'; 'tbr@hestia'
Subject: Re: gtlb drc'

vant wrote

>
>
>Tom,
> The gtlb drc run finished this morning. I started one up after the
>machine room came back up. There are 4 poly spacing errors and since I
>can't look at it from home, I don't know how severe it is. I expect
>these
>to be boundary errors only.
>
>If you want to start using the gtlb, I think it would be safe to do so.
>
>Eldred, if you want to see the errors, the error file is:
>
> /u/vanthof/compass/mobi/euterpe/gtlb.err
>
>Thanks,
>Dave

The results for the latest build .

/n/ghidra/s5/vo/euterpe/compass/save1/euterpe.ly
/n/ghidra/s5/vo/euterpe/compass/save1/chip_euterpe-iter.splvs

I noticed that you have a SHORT test running on euterpe , probably pointing at
compass/save , so I put all results in compass/save1 instead .

This version has cerberus , cdio , all the custom blocks except the plls .
There's one noconnect .

thanks

tvo

From: vant [vanthof@hestia]
Sent: Saturday, September 24, 1994 11:38 PM
To: 'Tom Vo'
Cc: 'vo@hestia'; 'bpw@hestia'; 'efelias@hestia'; 'hopper@hestia'; 'geert@hestia'; 'lisar@hestia'; 'tbr@hestia'
Subject: Re: glib drc'

Tom Vo writes:

>
>The results for the latest build .
>
>/n/ghidra/s5/vo/euterpe/compass/savel/euterpe.ly
>/n/ghidra/s5/vo/euterpe/compass/savel/chip_euterpe-iter.splvs

Thanks! I've started up a fullchip lvs and queued up the drc runs..

>
>I noticed that you have a SHORT test running on euterpe , probably
>pointing at compass/save , so I put all results in compass/savel
>instead
.

The shorts check was a vdd probe for Geert, however, it finished with a real short between vdd and vss. The problem is the probe run was not intended to find shorts, so none of the data was saved. I expect the lvs run to die because of this short, but I can at least extract and use that data.

>
>This version has cerberus , cdio , all the custom blocks except the
>pll's
.
>There's one noconnect .

Sounds like a bunch of stuff. Thanks,
Dave

--
Dave Van't Hof vanthof@microunity.com MicroUnity Systems Engineering,
Inc.
"What rolls down stairs, alone or in pairs, rolls over the neighbor's dog?"

What's great for a snack and fits on your back? It's log, log, log!"
LOG from BLAMMO! (tm) All kids love Log! #include
<std_disclaim.h>

From: Geert Rosseel [geert@rhea]
Sent: Saturday, September 24, 1994 11:47 PM
To: 'geert@rhea'
Subject: pager log message

page from geert to geert:
pageme gmake SL_HOME=/u/geert geert_euterpegards start:Sep_24_18:04 end:
Sep_24_21:45 exit 1

.

From: tbr
Sent: Sunday, September 25, 1994 12:17 AM
To: 'hopper'
Subject: planet warning
Follow Up Flag: Follow up
Flag Status: Red

Is this significant?

/n/auspex/s10/chip/euterpe/tools/bin/planet.ex: No physical size information available for :hr:

Tim

.

From: tbr
Sent: Sunday, September 25, 1994 12:22 AM
To: 'tom'; 'doi'
Cc: 'vanthof'
Subject: /n/tmp/chiplog/tbr.mothra.840.euterpe-verilog-bsrc-gf
Follow Up Flag: Follow up
Flag Status: Red

I have a .checkoutrc which does:

```
#!/bin/sh
```

```
#####  
# $Id: .checkoutrc,v 11.1 1994/09/24 21:24:40 LT tbr Exp $  
#####
```

```
dir=`pwd`  
sect=`basename $dir`  
gmake clean  
gmake GARDS_DISPLAY=clio:0.0 ${sect}gards 2>&1 > gards/makerrs  
status=$?  
cat gards/makerrs  
exit $status
```

when this ran it produced the file

```
/n/tmp/chiplog/tbr.mothra.840.euterpe-verilog-bsrc-gf
```

which appears to be garbled and at any rate nothing like the makerrs file that was left around. There are a couple of places where cat complains about a write error, which may have something to do with it. Another odd thing is that the chiplog file has a warning from topt:

Unknown command '\$' at line 1 while parsing power.tab.local. Ignoring...

which I can't see in the makerrs file! I'm certain it's genuine since I found the systax error. I have moved the makers file off to gf/gards/makerrs.840 so i can re-run if you want to take a look.

Tim

.

From: tbr
Sent: Sunday, September 25, 1994 2:19 AM
To: 'geert'
Cc: 'hardheads'
Subject: Makefile.rules
Follow Up Flag: Follow up
Flag Status: Red

I have released new versions of Makefile.defs and Makefile.rules which move all the remaining derived files into the gards subdirectory when running place/route jobs. To work with these new rules you will need to update your euterpe/verilog/bsrc/Makefile.share. Since some of the files required for the top level route are affected I am launching jobs to rebuild the released version in /u/chip.

If anyone has any trouble as a result of this release, please page me.

Tim

From: Tim B. Robinson [tbr@aphrodite]
Sent: Sunday, September 25, 1994 2:19 AM
To: 'geert@aphrodite'
Cc: 'hardheads@aphrodite'
Subject: Makefile.rules

I have released new versions of Makefile.defs and Makefile.rules which move all the remaining derived files into the gards subdirectory when running place/route jobs. To work with these new rules you will need to update your euterpe/verilog/bsrc/Makefile.share. Since some of the files required for the top level route are affected I am launching jobs to rebuild the released version in /u/chip.

If anyone has any trouble as a result of this release, please page me.

Tim

.

From: tbr
Sent: Sunday, September 25, 1994 2:39 AM
To: 'doi'
Subject: releasebom
Follow Up Flag: Follow up
Flag Status: Red

Can you account for why the higher level BOMS were 'unchanged' in this sequence?

```
tbr@gamorra ~/euterpe/verilog/bsrc/mc 713 % cvs ci -m 'force rebuild'
cvs commit: Examining .
cvs commit: Committing .
Checking in clean-request;
/u/chip/chip-archive/euterpe/verilog/bsrc/mc/clean-request,v <-- clean-request
new revision: 17.2; previous revision: 17.1
done
tbr@gamorra ~/euterpe/verilog/bsrc/mc 714 % releasebom -p -m 'force rebuild'
Releasing BOM in /n/auspex/s15/tbr/euterpe/verilog/bsrc/mc [New version 19.0]
Updating BOM in euterpe/verilog/bsrc [Version 128.12 (unchanged)]
Updating BOM in euterpe/verilog [Version 2.368 (unchanged)]
Updating BOM in euterpe [Version 2.502 (unchanged)]
tbr@gamorra ~/euterpe/verilog/bsrc/mc 715 %
```

.

From: Geert Rosseel [geert@ambiorix]
Sent: Sunday, September 25, 1994 10:33 AM
To: 'agc@ambiorix'; 'billz@ambiorix'; 'dickson@ambiorix'; 'hopper@ambiorix'; 'tbr@ambiorix';
'vo@ambiorix'; 'woody@ambiorix'
Subject: New toplevel place & route

Hi,

The latest toplevel run is in

~geert/chip/euterpe/verilog/bsrc/gards.save

It contains :

io0, hc0, hc1, gt, nb, cdio, drio, mst, rg, jc, iq, ctio0

-> 2.5 hours to route : 735 unrouted wires

-> bunch of HARD timing errors, I haven't looked at it yet

-> size grew from 169449 to 176489 atoms from -pass1 to -iter

This is probably because the blocks in /u/chip/ were run with
the temporary better timing numbers.

Geert

.

From: Geert Rosseel [geert@ambiorix]
Sent: Sunday, September 25, 1994 10:41 AM
To: 'geert@aphrodite'; 'tbr@aphrodite'
Cc: 'hardheads@aphrodite'
Subject: Re: Makefile.rules

How does this change affect Makefile and Makefile.tst in euterpe/verilog/bsrc ?

I was lucky. My large toplevel run finished about an hour before you made the changes. I was working in the section between icache and itag but I'm afraid I will have to rebuild these blocks locally again before I can make progress

Geert
d

.

From: tbr
Sent: Sunday, September 25, 1994 10:45 AM
To: 'Geert Rosseel'
Cc: 'geert@aphrodite'; 'hardheads@aphrodite'
Subject: Re: Makefile.rules
Follow Up Flag: Follow up
Flag Status: Red

Geert Rosseel wrote (on Sun Sep 25):

How does this change affect Makefile and Makefile.tst in euterpe/verilog/bsrc ?

I was lucky. My large toplevel run finished about an hour before you made the changes. I was working in the section between icache and itag but I'm afraid I will have to rebuild these blocks locally again before I can make progress

I looked around to see things were quite before launching it all.

You will need to update those Makefiles. I have only done minimal testing at that level. Main changes are

moved all control files (eg usepifpack) to the gards subdir.
renamed saved short nets file consistently to '<design>-base.short.nets'
Added support for two different power.tab.local files for blocks used twice

Expect some problems, but hopefully should be minor. I found and fixed the major problem with iteration, but it's still not working correctly for some reason, so I expect to have to change Makefile.rules again, but that should not reset anything.

Tim

.

From: Mark Hofmann [hopper@boreas]
Sent: Sunday, September 25, 1994 10:46 AM
To: 'Tim B. Robinson'
Subject: Re: NFS time warp

Tim B. Robinson writes:
[snip]

I ran the following:

```
tbr@gamorra ~/euterpe/verilog/bsrc/cdio 473 % rsh auspex date ; date ; touch foo ; touch gards/foo ; ls -ls foo gards/foo
Sat Sep 24 15:19:17 PDT 1994
Sat Sep 24 15:18:27 PDT 1994
0 -rw-rw-r-- 1 tbr      0 Sep 24 15:19 foo
0 -rw-rw-r-- 1 tbr      0 Sep 24 15:18 gards/foo
```

and indeed the date on gamorra is behind the date on the auspex and furthermore the files now look to have been created in the opposite order from what they really were.

Nice detective work, Tim!

How accurately is time supposed to be synced up between the machines?
Given the sizes of the files we are having to handle, symlinks are necessary (I have over 2GB linked this way in my euterpe tree onto local disks on gamorra and staypuft). If dates can only be guaranteed to a certain accuracy, we may have to insert sleep commands into the Makefile to try and deal with this.

Yow. I _thought_ clocks were supposed to be sync'ed better than this, but maybe the precision is really O(minutes). That would be unpleasant, to say the least. I hope the software types have a good answer.

-hopper

.

From: Mark Hofmann [hopper@boreas]
Sent: Sunday, September 25, 1994 10:51 AM
To: 'Tim B. Robinson'
Subject: Re: planet warning

Tim B. Robinson writes:

Is this significant?

/n/auspex/s10/chip/euterpe/tools/bin/planet.ex: No physical size information available for :hr:

Not significant, but I'll investigate what's going on. This information (if present) helps when planet produces a .pim file. This output is being used, at most, as a starting seed for mincut placement by alan.

-hopper

From: Mark Hofmann [hopper@boreas]
Sent: Sunday, September 25, 1994 11:00 AM
To: 'Geert Rosseel'
Cc: 'Tim B. Robinson'
Subject: Re: New toplevel place & route

Geert Rosseel writes:

The latest toplevel run is in

~geert/chip/euterpe/verilog/bsrc/gards.save

It contains :

io0, hc0, hc1, gt, nb, cdio, drio, mst, rg, jc, iq, ctio0

- > 2.5 hours to route : 735 unrouted wires
- > bunch of HARD timing errors, I haven't looked at it yet
- > size grew from 169449 to 176489 atoms from -pass1 to -iter
This ia probably because the blocks in /u/chip/ were run with
the temporary better timing numbers.

Okay. Do you know how many HARD errors there were?

Also, you should be able to add "ck"- though I'm having some trouble with the "clean-request" target when I releasebom to /u/chip. This is just a preliminary placement.

thanks,
-hopper

.

From: tbr
Sent: Sunday, September 25, 1994 11:03 AM
To: 'Mark Hofmann'
Cc: 'Geert Rosseel'
Subject: Re: New toplevel place & route
Follow Up Flag: Follow up
Flag Status: Red

Mark Hofmann wrote (on Sun Sep 25):

Geert Rosseel writes:

The latest toplevel run is in

`~geert/chip/euterpce/verilog/bsrc/gards.save`

It contains :

`io0, hc0, hc1, gt, nb, cdio, drio, mst, rg, jc, iq, ctio0`

- > 2.5 hours to route : 735 unrouted wires
- > bunch of HARD timing errors, I haven't looked at it yet
- > size grew from 169449 to 176489 atoms from -pass1 to -iter
This is probably because the blocks in /u/chip/ were run with the temporary better timing numbers.

Okay. Do you know how many HARD errors there were?

Also, you should be able to add "ck"- though I'm having some trouble with the "clean-request" target when I release bom to /u/chip. This is just a preliminary placement.

Watch out. There is still trouble with the new Makefile. I just got another typo out, but there is still a problem.

Tim

From: Tim B. Robinson [tbr@aphrodite]
Sent: Sunday, September 25, 1994 11:03 AM
To: 'Mark Hofmann'
Cc: 'Geert Rosseel'
Subject: Re: New toplevel place & route

Mark Hofmann wrote (on Sun Sep 25):

Geert Rosseel writes:

The latest toplevel run is in

~geert/chip/euterpe/verilog/bsrc/gards.save

It contains :

io0, hc0, hcl, gt, nb, cdio, drio, mst, rg, jc, iq, ctio0

-> 2.5 hours to route : 735 unrouted wires

-> bunch of HARD timing errors, I haven't looked at it yet

-> size grew from 169449 to 176489 atoms from -pass1 to -iter

This is probably because the blocks in /u/chip/ were run with
the temporary better timing numbers.

Okay. Do you know how many HARD errors there were?

Also, you should be able to add "ck"- though I'm having some trouble
with the "clean-request" target when I release bom to /u/chip. This is
just a preliminary placement.

Watch out. There is still trouble with the new Makefile. I just got another typo out,
but there is still a problem.

Tim

From: tbr
Sent: Sunday, September 25, 1994 11:10 AM
To: 'hopper'
Cc: 'brendan'
Subject: More Makefile wierdness
Follow Up Flag: Follow up
Flag Status: Red

Can you see anything wrong with the following:

```
$(NET_TRANSLATE) $(GARDS_DIR)/$.slack $(GARDS_DIR)/$.pass2.xrf | tr 'a-z' 'A-Z' | awk '{print $$1;}' >
$(GARDS_DIR)/ordered.all.nets
sort < $(GARDS_DIR)/$.short.nets > $(GARDS_DIR)/$.short.nets.tmp1
$(NET_TRANSLATE) $(GARDS_DIR)/$.slack $(GARDS_DIR)/$.pass2.xrf | tr 'a-z' 'A-Z' | sort > $(GARDS_DIR)/
$.short.nets.tmp2
join $(GARDS_DIR)/$.short.nets.tmp1 $(GARDS_DIR)/$.short.nets.tmp2 | sort +1 -n | awk '{print $$1;}' >
$(GARDS_DIR)/ordered.short.nets
rm -f $(GARDS_DIR)/$.short.nets.tmp1 $(GARDS_DIR)/$.short.nets.tmp2
```

When this bit of code gets executed I see:

```
HOME=/n/auspex/s15/tbr/euterpe/tools LM_LICENSE_FILE=/n/auspex/s15/tbr/euterpe/tools/sl/license/license.dat
DISPLAY=192.216.207.9:0.0 SL_TOTAL_DURATION=500
CHIPROOT=/n/auspex/s15/tbr/euterpe /n/auspex/s15/tbr/euterpe/tools/bin/net_translate gards/io0.slack gards/io0-pass1.xrf |
tr 'a-z' 'A-Z' | awk '{print $1;}' > gards/ordered.all.nets
Scanning "gars/io0-pass1.xrf"... *WARNING* - net map not found in xrf file: "gars/io0-pass1.xrf"
0 netname translations found in "gars/io0-pass1.xrf"
935 names passed through unaltered
sort < gards/io0.short.nets > gards/io0.short.nets.tmp1
HOME=/n/auspex/s15/tbr/euterpe/tools LM_LICENSE_FILE=/n/auspex/s15/tbr/euterpe/tools/sl/license/license.dat
DISPLAY=192.216.207.9:0.0 SL_TOTAL_DURATION=500
CHIPROOT=/n/auspex/s15/tbr/euterpe /n/auspex/s15/tbr/euterpe/tools/bin/net_translate gards/io0.slack gards/io0-pass1.xrf |
tr 'a-z' 'A-Z' | sort > gards/io0.short.nets.tmp2
Scanning "gars/io0-pass1.xrf"... *WARNING* - net map not found in xrf file: "gars/io0-pass1.xrf"
0 netname translations found in "gars/io0-pass1.xrf"
935 names passed through unaltered
join gards/io0.short.nets.tmp1 $(GARDS_DIR)/$.short.nets.tmp2 | sort +1 -n | awk '{print $1;}' > gards/ordered.short.nets
/bin/sh: syntax error at line 1: `(' unexpected
gmake[2]: *** [gars/io0-iter.sdl] Error 2
```

Notice that one instance of \$(GARDS_DIR) has not been substituted by make, and the \$* following it got changed just to *. I just can't find anything different about that instance.

.

From: tbr
Sent: Sunday, September 25, 1994 11:21 AM
To: 'Mark Hofmann'
Subject: euterpe/verilog/bsrc euterpe.V euterpe_driver.V euterpe_wrap.V
Follow Up Flag: Follow up
Flag Status: Red

Mark Hofmann wrote (on Sun Sep 25):

Update of /p/cvsroot/euterpe/verilog/bsrc
In directory nosferatu:/N/auspex/root/s32/hopper/chip/euterpe/verilog/bsrc

Modified Files:
euterpe.V euterpe_driver.V euterpe_wrap.V

Log Message:
changed ctiod ->ctio0, ctioi -> ctio1, ck_fgen -> ck_ck (latter is
gratuitous and silly. I was debugging a problem and thought "fgen"
was causing difficulties).

Can you make sure the Makefile exclude lists are updated to mach the
new intance names please?

Tim

.

From: Mark Hofmann [hopper@boreas]
Sent: Sunday, September 25, 1994 11:25 AM
To: 'Tim B. Robinson'
Subject: Re: euterpe/verilog/bsrc euterpe.V euterpe_driver.V euterpe_wrap.V

Tim B. Robinson writes:

Mark Hofmann wrote (on Sun Sep 25):

Update of /p/cvsroot/euterpe/verilog/bsrc
In directory nosferatu:/N/auspex/root/s32/hopper/chip/euterpe/verilog/bsrc

Modified Files:
euterpe.V euterpe_driver.V euterpe_wrap.V

Log Message:
changed ctiod -> ctio0, ctioi -> ctio1, ck_fgen -> ck_ck (latter is
gratuitous and silly. I was debugging a problem and thought "fgen"
was causing difficulties).

Can you make sure the Makefile exclude lists are updated to match the
new instance names please?

Okay. I had already done this.
Can I release both the euterpe.*V files ?

-hopper

.

From: tbr
Sent: Sunday, September 25, 1994 11:25 AM
To: 'Mark Hofmann'
Subject: Re: euterpe/verilog/bsrc euterpe.V euterpe_driver.V euterpe_wrap.V
Follow Up Flag: Follow up
Flag Status: Red

Mark Hofmann wrote (on Sun Sep 25):

Tim B. Robinson writes:
Can you make sure the Makefile exclude lists are updated to match the
new intance names please?

I believe I have already done that. I'll just make sure.

Great, thanks.

Tim

.

From: tbr
Sent: Sunday, September 25, 1994 11:29 AM
To: 'Mark Hofmann'
Subject: Re: euterpe/verilog/bsrc euterpe.V euterpe_driver.V euterpe_wrap.V
Follow Up Flag: Follow up
Flag Status: Red

Mark Hofmann wrote (on Sun Sep 25):

Tim B. Robinson writes:

Mark Hofmann wrote (on Sun Sep 25):

Update of /p/cvsroot/euterpe/verilog/bsrc
In directory nosferatu:/N/auspex/root/s32/hopper/chip/euterpe/verilog/bsrc

Modified Files:
euterpe.V euterpe_driver.V euterpe_wrap.V

Log Message:
changed ctiod ->ctio0, ctioi -> ctio1, ck_fgen -> ck_ck (latter is
gratuitous and silly. I was debugging a problem and thought "fgen"
was causing difficulties).

Can you make sure the Makefile exclude lists are updated to mach the
new intance names please?

Okay, I had already done this.
Can I releasebom the euterpe.*V files ?

Probably best not to. As soon as I have all this placement stuff
stable again, we need to make a full .0 BOM again in bsrc for verification.
I think we should avoid releasing individual files. Geert can always
pick them up with an update if he needs them fo the top level route
expt.

.

From: Mark Hofmann [hopper@boreas]
Sent: Sunday, September 25, 1994 11:31 AM
To: 'Tim B. Robinson'
Subject: Re: euterpe/verilog/bsrc euterpe.V euterpe_driver.V euterpe_wrap.V

Tim B. Robinson writes:

Can I releasebom the euterpe.*V files ?

Probably best not to. As soon as I have all this placement stuff stable again, we need to make a full .0 BOM again in bsrc for verification. I think we should avoid releasing individual files. Geert can always pick them up with an update if he needs them fo the top level route expt.

Okay, fine.

thanks,
-hopper

.

From: tbr
Sent: Sunday, September 25, 1994 11:34 AM
To: 'hopper'
Cc: 'ericm'; 'brendan'
Subject: Makefile problem
Follow Up Flag: Follow up
Flag Status: Red

Can you forward that mail al sent you about the make not expanding the variable to eric please?

The exact same thing has just happened in the release process (this time on godzilla. I haven't a clue what it can be, but here's the log this time:

```
HOME=/n/auspex/s10/chip/euterpe/tools LM_LICENSE_FILE=/n/auspex/s10/chip/euterpe/tools/sl/license/license.dat
DISPLAY=clio:0.0 SL_TOTAL_DURATION=500
CHIPROOT=/n/auspex/s10/chip/euterpe /n/auspex/s10/chip/euterpe/tools/bin/net_translate gards/io0.slack gards/io0-
pass1.xrf | tr 'a-z' 'A-Z' | awk '{print $1;}' > gards/ordered.all.nets
sort < gards/io0.short.nets > gards/io0.short.nets.tmp1
HOME=/n/auspex/s10/chip/euterpe/tools LM_LICENSE_FILE=/n/auspex/s10/chip/euterpe/tools/sl/license/license.dat
DISPLAY=clio:0.0 SL_TOTAL_DURATION=500
CHIPROOT=/n/auspex/s10/chip/euterpe /n/auspex/s10/chip/euterpe/tools/bin/net_translate gards/io0.slack gards/io0-
pass1.xrf | tr 'a-z' 'A-Z' | sort > gards/io0.short.nets.tmp2
join gards/io0.short.nets.tmp1 ${GARDS_DIR}/*.short.nets.tmp2 | sort +1 -n | awk '{print $1;}' > gards/ordered.short.nets
gmake[2]: Leaving directory `/N/auspex/root/s10/chip/euterpe/verilog/bsrc/io'
```

However, this time I don't see the message from the shell complaining about the syntax error.

Tim

.

From: Mark Hofmann [hopper@boreas]
Sent: Sunday, September 25, 1994 11:52 AM
To: 'Tim B. Robinson'
Subject: Re: Makefile problem

Tim B. Robinson writes:

Can you forward that mail aI sent you about the make not expanding the variable to eric please?

The exact same thing has just happened in the release process (this time on godzilla. I haven't a clue what it can be, but here's the log this time:

```
HOME=/n/auspex/s10/chip/euterpe/tools LM_LICENSE_FILE=/n/auspex/s10/chip/euterpe/tools/sl/license/license.dat
DISPLAY=clio:0.0 SL_TOTAL_DURATION=500
CHIPROOT=/n/auspex/s10/chip/euterpe /n/auspex/s10/chip/euterpe/tools/bin/net_translate gards/io0.slack gar ds/io0-
pass1.xrf | tr 'a-z' 'A-Z' | awk '{print $1;}' > gards/ordered.all.nets
sort < gards/io0.short.nets > gards/io0.short.nets.tmp1
HOME=/n/auspex/s10/chip/euterpe/tools LM_LICENSE_FILE=/n/auspex/s10/chip/euterpe/tools/sl/license/license.dat
DISPLAY=clio:0.0 SL_TOTAL_DURATION=500
CHIPROOT=/n/auspex/s10/chip/euterpe /n/auspex/s10/chip/euterpe/tools/bin/net_translate gards/io0.slack gar ds/io0-
pass1.xrf | tr 'a-z' 'A-Z' | sort > gards/io0.short.nets.tmp2
join gards/io0.short.nets.tmp1 ${GARDS_DIR}/*.short.nets.tmp2 | sort +1 -n | awk '{print $1;}' > gards/ordered.short.nets
gmake[2]: Leaving directory '/N/auspex/root/s10/chip/euterpe/verilog/bsrc/io'
```

However, this time I don't see the message from the shell complaining about the syntax error.

Sorry, after I looked at the mail and couldn't see any difference between the lines in the script I cleaned up my mailbox! So I don't have a copy to forward on.

-hopper

From: tbr
Sent: Sunday, September 25, 1994 12:02 PM
To: 'ericm'
Subject: forwarded message from tbr
Follow Up Flag: Follow up
Flag Status: Red

For reference, here's the previous mail. I re-ran the exact same make on the same machine with nothing changed and it went to completion. Then, when I released the stuff and it tried to build the reference version in /u/chip, the same problem re-appeared.

----- Start of forwarded message -----

To: hopper
cc: brendan
Subject: More Makefile weirdness

Can you see anything wrong with the following:

```
$(NET_TRANSLATE) $(GARDS_DIR)/$*.slack $(GARDS_DIR)/$*-pass2.xrf | tr 'a-z' 'A-Z' | awk '{print $$1;}' >
$(GARDS_DIR)/ordered.all.nets
sort < $(GARDS_DIR)/$*.short.nets > $(GARDS_DIR)/$*.short.nets.tmp1
$(NET_TRANSLATE) $(GARDS_DIR)/$*.slack $(GARDS_DIR)/$*-pass2.xrf | tr 'a-z' 'A-Z' | sort > $(GARDS_DIR)/
$*.short.nets.tmp2
join $(GARDS_DIR)/$*.short.nets.tmp1 $(GARDS_DIR)/$*.short.nets.tmp2 | sort +1 -n | awk '{print $$1;}' >
$(GARDS_DIR)/ordered.short.nets
rm -f $(GARDS_DIR)/$*.short.nets.tmp1 $(GARDS_DIR)/$*.short.nets.tmp2
```

When this bit of code gets executed I see:

```
HOME=/n/auspex/s15/tbr/euterpe/tools LM_LICENSE_FILE=/n/auspex/s15/tbr/euterpe/tools/sl/license/license.dat
DISPLAY=192.216.207.9:0.0 SL_TOTAL_DURATION=500
CHIPROOT=/n/auspex/s15/tbr/euterpe /n/auspex/s15/tbr/euterpe/tools/bin/net_translate gards/io0.slack gards/io0-pass1.xrf |
tr 'a-z' 'A-Z' | awk '{print $1;}' > gards/ordered.all.nets
Scanning "gars/io0-pass1.xrf"... *WARNING* - net map not found in xrf file: "gars/io0-pass1.xrf"
0 netname translations found in "gars/io0-pass1.xrf"
935 names passed through unaltered
sort < gards/io0.short.nets > gards/io0.short.nets.tmp1
HOME=/n/auspex/s15/tbr/euterpe/tools LM_LICENSE_FILE=/n/auspex/s15/tbr/euterpe/tools/sl/license/license.dat
DISPLAY=192.216.207.9:0.0 SL_TOTAL_DURATION=500
CHIPROOT=/n/auspex/s15/tbr/euterpe /n/auspex/s15/tbr/euterpe/tools/bin/net_translate gards/io0.slack gards/io0-pass1.xrf |
tr 'a-z' 'A-Z' | sort > gards/io0.short.nets.tmp2
Scanning "gars/io0-pass1.xrf"... *WARNING* - net map not found in xrf file: "gars/io0-pass1.xrf"
0 netname translations found in "gars/io0-pass1.xrf"
935 names passed through unaltered
join gards/io0.short.nets.tmp1 $(GARDS_DIR)/$*.short.nets.tmp2 | sort +1 -n | awk '{print $1;}' > gards/ordered.short.nets
/bin/sh: syntax error at line 1: `(' unexpected
gmake[2]: *** [gars/io0-iter.sdl] Error 2
```

Notice that one instance of \$(GARDS_DIR) has not been substituted by make, and the \$* following it got changed just to *. I just can't find anything different about that instance.

----- End of forwarded message -----

.

From: Mark Hofmann [hopper@boreas]
Sent: Sunday, September 25, 1994 12:07 PM
To: 'Tim B. Robinson'
Subject: output of euterpe/verilog/bsrc/ck/.checkoutrc (fwd)

Hi Tim,

When I release "ck" I get the following, (but it builds fine locally).
Can you see what's wrong?

-thanks,
hopper

Buffalo Chip writes:
To: hopper@nosferatu
Subject: output of euterpe/verilog/bsrc/ck/.checkoutrc

Sun Sep 25 09:33:50 PDT 1994 (hopper Sun, 25 Sep 1994 09:33:27 -0700) euterpe/verilog/bsrc/ck
[Release BOM (V13.0) in euterpe/verilog/bsrc/ck (Sun Sep 25 09:33:50 PDT 1994)]

```
Dir    euterpe/verilog/bsrc/ck          BOM 13.0
10.1   .checkoutrc
1.6    Makefile
9.1    ck.V
1.3    cktop.V
11.1   clean
12.1   clean-request                    (No)
10.1   genpim.pl
10.4   pimlib.pl
====> running euterpe/verilog/bsrc/ck/.checkoutrc (Sun Sep 25 09:33:56 PDT 1994) <===
rm -f *.eqn *.esp *.opt *.optesp *.v *.tmp* *.warn *.plat
rm -f *.pim.* doespresso.*
rm -f *.v *.v2e *.log vfiles v2e.* verilog.*
rm -f *.edif *.topt.log *.stat *.loads *.instances *.size
rm -f topt.log emerge.tab power.tab
rm -f usepifpack usespartiles usepadtiles addclock nopgroute noobs
rm -f gards/*
rm -f *-pass* *-iter* *-base* *.short.nets
rm -f makerrs tmp1 tmp2
touch clean
gmake[2]: *** No rule to make target `gards/ck-pass2.sdl'.
gmake[1]: *** [ck-base.netcap] Error 1
gmake[1]: Target `gards/ck-iter' not remade because of errors.
gmake: *** [ckgards] Error 1
#
# turn off pgroute
#
[ -f gards/nopgroute ] || touch gards/nopgroute
#
# use padtiles
#
[ -f gards/usepadtiles ] || touch gards/usepadtiles
#
# use pifpack
#
[ -f gards/usepifpack ] || touch gards/usepifpack
```

```

#
# insert an instance of the clock tree
#
[ -f gards/addclock ] || touch gards/addclock
#
# disable old dcell placement obstruction
#
[ -f gards/noobs ] || touch gards/noobs
#
# now do it . . .
#
gmake GARDS_DISPLAY=clio:0.0 gards/ck-iter
gmake[1]: Entering directory `/N/auspex/root/s10/chip/euterpe/verilog/bsrc/ck'
cat /n/auspex/s10/chip/euterpe/proteus/verilog/diff.h ck.V | /lib/cpp -P -C -B | sed -e '/^$/d'> ck.v.tmp
mv ck.v.tmp ck.v
echo ck.v | tr '\012'> vfiles

cat /n/auspex/s10/chip/euterpe/proteus/verilog/dxlib/xlib.config /n/auspex/s10/chip/euterpe/proteus/verilog/dclib/clib.config /r
> gards/ck.v2e.config
#
# Take a snooze to make sure vfiles looks older than the .v2e file
# when they are on different NFS file systems
#
sleep 60
CHIPROOT=/n/auspex/s10/chip/euterpe /n/auspex/s10/chip/euterpe/tools/bin/v2e -host nosferatu -f vfiles -o gards/ck.v2e -
c gards/ck.v2e.config -l gards/ck.v2e.log -y ./io -y /n/auspex/s10/chip/euterpe/proteus/verilog/mlib +libext+.v -
y /n/auspex/s10/chip/ euterpe/proteus/verilog/dxlib -y /n/auspex/s10/chip/euterpe/proteus/verilog/dclib -
y /n/auspex/s10/chip/euterpe/proteus/verilog/delib
V2E 1.0a Sep 25, 1994 09:35:10
* Copyright Cadence Design Systems Inc. 1990. *
* All Rights Reserved. Licensed Software. *
* Confidential and proprietary information which is the *
* property of Cadence Design Systems Inc. *
Compiling source file "ck.v"
Scanning library directory "./io"
Scanning library directory "/n/auspex/s10/chip/euterpe/proteus/verilog/mlib"
Scanning library directory "/n/auspex/s10/chip/euterpe/proteus/verilog/dxlib"
Scanning library directory "/n/auspex/s10/chip/euterpe/proteus/verilog/dclib"
Warning! library directory "/n/auspex/s10/chip/euterpe/proteus/verilog/delib" was specified but not needed.
"ck.v", 20: warning! following implicit wire has no fanin
ck.reset
"ck.v", 20: warning! following implicit wire has no fanin
ck.reset_n
"ck.v", 21: warning! following implicit wire has no fanin
ck.clk54_a2p
"ck.v", 21: warning! following implicit wire has no fanin
ck.clk54_b2p
"ck.v", 21: warning! following implicit wire has no fanin
ck.rst3
"ck.v", 21: warning! following implicit wire has no fanin
ck.rst3_n
"ck.v", 23: warning! following implicit wire has no fanin
ck.okx_n
"ck.v", 23: warning! following implicit wire has no fanin
ck.rst4
"ck.v", 23: warning! following implicit wire has no fanin
ck.rst4_n
"ck.v", 24: warning! following implicit wire has no fanin
ck.q2_n
"ck.v", 24: warning! following implicit wire has no fanin
ck.q0sa_n

```

```

"ck.v", 24: warning! following implicit wire has no fanin
ck.q0sa
"ck.v", 26: warning! following implicit wire has no fanin
ck.q0
"ck.v", 26: warning! following implicit wire has no fanin
ck.q0_n
"ck.v", 28: warning! following implicit wire has no fanin
ck.dq0
"ck.v", 28: warning! following implicit wire has no fanin
ck.dq0_n
"ck.v", 30: warning! following implicit wire has no fanin
ck.q1_n
"ck.v", 30: warning! following implicit wire has no fanin
ck.q1
"ck.v", 32: warning! following implicit wire has no fanin
ck.dq1_n
"ck.v", 32: warning! following implicit wire has no fanin
ck.dq1
"ck.v", 34: warning! following implicit wire has no fanin
ck.q2
"ck.v", 35: warning! following implicit wire has no fanin
ck.pu
"ck.v", 35: warning! following implicit wire has no fanin
ck.pd
"ck.v", 39: warning! following implicit wire has no fanin
ck.oka_n
"ck.v", 39: warning! following implicit wire has no fanin
ck.oka
"ck.v", 40: warning! following implicit wire has no fanin
ck.okb_n
"ck.v", 40: warning! following implicit wire has no fanin
ck.okb
"ck.v", 41: warning! following implicit wire has no fanin
ck.okc_n
"ck.v", 41: warning! following implicit wire has no fanin
ck.okc
"ck.v", 42: warning! following implicit wire has no fanin
ck.okx

```

Highest level modules:

ck

Reading configuration file gards/ck.v2e.config

Processing configuration file

Translating Verilog source

Writing output to gards/ck.v2e

0 warnings 0 errors

End of V2E 1.0a Sep 25, 1994 09:35:14

rm -f gards/ck.emerge.tab

cp /n/auspex/s10/chip/euterpe/teutis/misc/emerge.tab gards/ck.emerge.tab.tmp

chmod +w gards/ck.emerge.tab.tmp

```

awk '{if($1 == "N") print "createport top", $2, "input"; \
if($1 == "N") print "addportproperty top", $2, "GARDS_SAVE";}' \
/n/auspex/s10/chip/euterpe/compass/baseplate/toplabel.ly | sed 's/"/"/g' >> gards/ck.emerge.tab.tmp
sed -e 's/(...)[(\\)]/1<2>/' < gards/ck.emerge.tab.tmp > gards/ck.emerge.tab
rm -f gards/ck.emerge.tab.tmp

```

```

CHIPROOT=/n/auspex/s10/chip/euterpe /n/auspex/s10/chip/euterpe/tools/bin/emerge -f -R -p gards/ck.emerge.tab -c
gards/ck.v2e -o gards/ck.edif -O gards/ck.emerge.log -I ./cg/cgclockbias.v2e cgclockbias

```

Running emerge compiled on Sun Sep 25 06:02:39 GMT 1994

Consuming edif file gards/ck.v2e


```
Found edif structure: CK_46_V2E
Flattening edif;
flattened 20 instances; created 17 nets in CK_46_V2E
Reading Edif file for instance placement: ../cg/cgclockbias.v2e
Consuming power table information file gards/ck.emerge.tab
Performing Edif Transformations...
Disgorging edif file gards/ck.edif
Writing edif structure: gards_47_ck_46_edif
Memory usage: 0.246MB
/usr/local/bin/perl genpim.pl > pim.tmp
mv pim.tmp gards/ck-pass1.pim
#
# Get an initial sdl file. A manhattan approximation will be used
#
gmake GARDS_DISPLAY=clio:0.0 CYCLETIME=895 gards/ck-pass2.sdl
gmake[2]: Entering directory `/N/auspex/root/s10/chip/euterpe/verilog/bsrc/ck'
gmake[2]: Leaving directory `/N/auspex/root/s10/chip/euterpe/verilog/bsrc/ck'
gmake[1]: Leaving directory `/N/auspex/root/s10/chip/euterpe/verilog/bsrc/ck'
[finished at Sun Sep 25 09:35:22 PDT 1994 -- exit status 1]
```

.

From: tbr
Sent: Sunday, September 25, 1994 12:13 PM
To: 'Mark Hofmann'
Subject: output of euterpe/verilog/bsrc/ck/.checkoutrc (fwd)
Follow Up Flag: Follow up
Flag Status: Red

Mark Hofmann wrote (on Sun Sep 25):

Hi Tim,

When I release "ck" I get the following, (but it builds fine locally).
Can you see what's wrong?

Do you have a power.tab.local? I don't see one checked in.

If that's it, you can either add a dummy file, or put the following in
the Makefile

```
$(GARDS_DIR)/ck.power.tab.local:  
touch $@
```

Tim

.

From: Mark Hofmann [hopper@boreas]
Sent: Sunday, September 25, 1994 12:16 PM
To: 'Tim B. Robinson'
Subject: Re: output of euterpe/verilog/bsrc/ck/.checkoutrc (fwd)

Tim B. Robinson writes:

Do you have a power.tab.local? I don't see one checked in.

If that's it, you can either add a dummy file, or put the following in the Makefile

```
$(GARDS_DIR)/ck.power.tab.local:  
touch $@
```

I think that's it. I'm releasing now...

-hopper

.

From: tbr
Sent: Sunday, September 25, 1994 1:33 PM
To: 'doi'
Subject: chipq
Follow Up Flag: Follow up
Flag Status: Red

I still see it report 0:59 right after it starts a job:

	ID	Target Directory	Machine(pid)	Who	Stat
1	591	proteus/leafgen	staypuft(2673)	brianl	4:10
2	599	euterpe/verilog/bsrc/io	godzilla(8412)	tbr	1:44
3	602	euterpe/verilog/bsrc/mst	medusa(2395)	tbr	0:25
4	604	euterpe/verilog/bsrc/mc	ghidra(15767)	tbr	0:59

.

From: vant [vanthof@hestia]
Sent: Sunday, September 25, 1994 1:44 PM
To: 'Mark Hofmann'
Cc: 'Tim B. Robinson'; 'Dave Van't Hof'
Subject: Re: Tomato dead?

Mark Hofmann writes:

>
>Tim B. Robinson writes:
>
> Dave had a DRC run on it earlier in the evening. That may have been
> an important one, so you may want to check with him. Right now most
> machines are idle. Let's hang on till either we confirm we need it
> for an important DRC, or else all the others get loaded up.
>
>Okay. Dave- do we need tomato up for DRCs?
>
>-thanks,
> hopper
>

Yes, it was important. One of the euterpe fullchip drc runs, either upper
or lower, I don't remember.
Dave

--
Dave Van't Hof vanthof@microunity.com MicroUnity Systems Engineering, Inc.
"What rolls down stairs, alone or in pairs, rolls over the neighbor's dog?
What's great for a snack and fits on your back? It's log, log, log!"
LOG from BLAMMO! (tm) All kids love Log! #include <std_disclaim.h>

From: vant [vanthof@hestia]
Sent: Sunday, September 25, 1994 1:56 PM
To: 'Fred Obermeier'; 'Geert Rossee'
Cc: 'Dave Van't Hof'; 'Mark Hofmann'; 'Tim B. Robinson'; 'Lisa Robinson'; 'Tom Vo'
Subject: orchistmp metals drc

The orchistmp drc's finished and there are some errors.

The error file is in
/u/vanthof/compass/mobi/orchis/tapeout/orchistmp_upper.err

The suspicious errors are the metal s2 spacing violations. I have not looked at these yet as I can't from home.

Thanks,
Dave

--

Dave Van't Hof vanthof@microunity.com MicroUnity Systems Engineering,
Inc.

"What rolls down stairs, alone or in pairs, rolls over the neighbor's dog?"

What's great for a snack and fits on your back? It's log, log, log!"

LOG from BLAMMO! (tm) All kids love Log! #include
<std_disclaim.h>

.

From: Lisa Robinson [lisar@nosferatu]
Sent: Sunday, September 25, 1994 4:37 PM
To: 'mws@nosferatu'; 'jeffm@nosferatu'
Cc: 'dickson@nosferatu'; 'tbr@nosferatu'
Subject: bback of cyl 0 problem

Dump in /n/rhodan/s3/euterpe/verilog/bsrc/test15.*

Lisa R.

From: John Campbell [solo@echidna]
Sent: Sunday, September 25, 1994 6:01 PM
To: 'Warren R. Ong'
Cc: 'Mark Hofmann'; 'Dave Van't Hof'; 'Thomas Laidig'; 'Geert Rosseel'
Subject: ea..mumble.lvs

Sep 19 15:48 /u/chip/euterpe/proteus/compass/layouts/ealnf36s9x4a.ly
Sep 15 10:40
/n/auspex/s10/chip/euterpe/proteus/ged/ea/ealnf36s9x4a/spice_cn.1.1

looks like someone introduced a few changes in this one. maybe they were less than perfect. let's look tomorrow.

....
regards,
solo a.k.a. John Campbell x516

.

From: Mark Hofmann [hopper@boreas]
Sent: Sunday, September 25, 1994 9:28 PM
To: 'Tim B. Robinson'
Cc: 'Richard Dickson'
Subject: Re: ck section

Tim B. Robinson writes:

There is a problem with whatever renaming has been done. I can't get the top level to compile. What is the correct module name to be instantiated at the top level after you latest changes?

Okay. I probably screwed up. I think the module name was "ck_fgen" and I changed it to "ck_ck" in cktop.V and also in euterpe.V (the latter checked in, but not released). Let me know what I need to change or, feel free to change it as you need.

-hopper

.

From: tbr
Sent: Sunday, September 25, 1994 9:43 PM
To: 'Mark Hofmann'
Cc: 'Richard Dickson'
Subject: Re: ck section
Follow Up Flag: Follow up
Flag Status: Red

Mark Hofmann wrote (on Sun Sep 25):

Tim B. Robinson writes:

There is a problem with whatever renaming has been done. I can't get the top level to compile. What is the correct module name to be instantiated at the top level after you latest changes?

Okay. I probably screwed up. I think the module name was "ck_fgen" and I changed it to "ck_ck" in cktop.V and also in euterpe.V (the latter checked in, but not released). Let me know what I need to change or, feel free to change it as you need.

I fixed it. It seem to need to be just 'ck' which is consisten with the module name having to match the section name. I have released a new top level BOM which brings everything up to date except cc.

Tim

From: Richard Dickson [dickson@demeter]
Sent: Sunday, September 25, 1994 11:04 PM
To: 'tbr@demeter'
Subject: xlu

tim,

there was a csyn error that tom vo fixed in the xlu last time around.
error (DiffInputNodePairCheck.755) in file "tbr_euterpe-pass1.splvs": leaf-inp
ut differential is missing a complementary leaf-input

instance path: top.xxlug_ctrldatag_q_9ag_q_9a_42_106p7p_1.xlrsltr9_42
cellname path: top.scsmf3rv3.is3_ad1ph

instance path: top.xxlug_ctrldatag_q_9ag_q_9a_62_126p9p_1.xlrsltr9_n_62
cellname path: top.scsmf3v3.sis1_ad1ph

dickson

.

From: tbr
Sent: Sunday, September 25, 1994 11:06 PM
To: 'Richard Dickson'
Cc: 'vo'; 'hopper'
Subject: xlu
Follow Up Flag: Follow up
Flag Status: Red

Richard Dickson wrote (on Sun Sep 25):

tim,

there was a csyn error that tom vo fixed in the xlu last time around.
error (DiffInputNodePairCheck.755) in file "tbr_euterpe-pass1.splvs": leaf-inp
ut differential is missing a complementary leaf-input

instance path: top.xxlug_ctrldatag_q_9ag_q_9a_42_106p7p_1.xlrsltr9_42
cellname path: top.scsmf3rv3.is3_ad1ph

instance path: top.xxlug_ctrldatag_q_9ag_q_9a_62_126p9p_1.xlrsltr9_n_62
cellname path: top.scsmf3v3.sis1_ad1ph

dickson

Do you know what he fixed? I think I have the latest schematics etc
(I'll double check).

Tim

.

From: tbr
Sent: Sunday, September 25, 1994 11:56 PM
To: 'vant'
Cc: 'bill@aphrodite'; 'dickson@aphrodite'; 'fwo@aphrodite'; 'vanthof@aphrodite'
Subject: Re: topt swing checks
Follow Up Flag: Follow up
Flag Status: Red

vant wrote (on Sun Sep 25):

Tim B. Robinson writes:

>
>For now I am only running the first pass (since we don't have a full
>route), then runnign it through the pass that converts the strength
>file to an edif file. I get exit status 4 on the first run and 0 (not
>forced) on the second.
>
>Tim
>

Hmm. that doesn't sound right. I'll look into it. topt should consistantly
report the same errors for each run.

Bear in mind that on the second run we don't even give a -p option, so
it's not doing very much. Here is the command:

```
CHIPROOT=/n/auspex/s15/tbr/euterpe /n/auspex/s15/tbr/euterpe/tools/bin/topt -e gards/tbr_euterpe.edif -o gards/tbr_euterpe-  
pass1.edif.tmp -g /n/auspex/s15/tbr/euterpe/proteus/leafgen/toptList -g /n/auspex/s15/tbr/euterpe/proteus/exlax/toptList -  
g /n/auspex/s15/tbr/euterpe/proteus/custom/toptList \  
-A /n/auspex/s15/tbr/euterpe/proteus/leafgen/caps/cap.lib -A /n/auspex/s15/tbr/euterpe/proteus/exlax/caps/cap.lib -  
A /n/auspex/s15/tbr/euterpe/proteus/custom/caps/cap.lib -K gards/tbr_euterpe-pass1.strength -E vref_0ph -0
```

.

From: tbr
Sent: Monday, September 26, 1994 3:08 AM
To: 'hopper'; 'wingard'
Cc: 'vanthof'
Subject: LVS netlist
Follow Up Flag: Follow up
Flag Status: Red

My attempt to get a top level LVS netlist seems to have died with:

MicroUnity Spice Interface run on Sep 25 22:0:33 1994
DESIGN NAME : 'TBR_EUTERPE_PASS1'
DESIGN COMPILATION ON Sep 25 22:0:39 1994

No error detected
1 oversights detected
52 warnings detected

cpu time 0:26:44
elapsed time 2:23:01

****ERROR**** in <stdin>(34): match failed for instance card: [xr in out 0.050]

Any idea what this could mean? peppermill is still grinding, but I've not seen this output before. There is nothing else indicating an error.

Tim

.

From: tbr
Sent: Monday, September 26, 1994 8:12 AM
To: 'dickson'
Subject: csyn
Follow Up Flag: Follow up
Flag Status: Red

Output from the latest run in

~tbr/euterpe/verilog/bsrc/tbr_euterpe-pass1.csyn

We are down to 81K. There should be stuff in there still about the
0p/1p problem on the XLU output.

Tim

.

From: vant [vanthof@hestia]
Sent: Monday, September 26, 1994 8:17 AM
To: 'Tim B. Robinson'
Cc: 'hopper@aphrodite'; 'wingard@aphrodite'; 'vanthof@aphrodite'
Subject: Re: LVS netlist

Tim B. Robinson writes:

>
>
>My attempt to get a top level LVS netlist seems to have died with:
>
>MicroUnity Spice Interface run on Sep 25 22:0:33 1994
> DESIGN NAME : 'TBR_EUTERPE_PASS1'
> DESIGN COMPILATION ON Sep 25 22:0:39 1994
>
>
>No error detected
> 1 oversights detected
> 52 warnings detected
>
>cpu time 0:26:44
>elapsed time 2:23:01
>
>**ERROR** in <stdin>(34): match failed for instance card: [xr in out 0.050]
>
>Any idea what this could mean? peppermill is still grinding, but I've
>not seen this output before. There is nothing else indicating an
>error.
>
>Tim
>

That's a peppermill error. When it displays teh 'cpu time x:xx:xx', then the spice.ex phase is complete.

The error being displayed is for a 'shorting resistor' which is used to replace objects like 0 volt voltage regulators (to measure current).

I'll have to take a look at the intermediate spice netlist to track this down.

Dave

--
Dave Van't Hof vanthof@microunity.com MicroUnity Systems Engineering, Inc.
"What rolls down stairs, alone or in pairs, rolls over the neighbor's dog?
What's great for a snack and fits on your back? It's log, log, log!"
LOG from BLAMMO! (tm) All kids love Log! #include <std_disclaim.h>

From: tbr
Sent: Monday, September 26, 1994 8:27 AM
To: 'vant'
Cc: 'hopper@aphrodite'; 'vanthof@aphrodite'; 'wingard@aphrodite'
Subject: Re: LVS netlist
Follow Up Flag: Follow up
Flag Status: Red

vant wrote (on Mon Sep 26):

Tim B. Robinson writes:

>
>
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>
>MicroUnity Spice Interface run on Sep 25 22:0:33 1994
> DESIGN NAME : 'TBR_EUTERPE_PASS1'
> DESIGN COMPILATION ON Sep 25 22:0:39 1994
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>
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The error being displayed is for a 'shorting resistor' which is used to replace objects like 0 volt voltage regulators (to measure current).

I'll have to take a look at the intermediate spice netlist to track this

Well, it actually completed and I have a csyn result. It's looking good, we are down to 81K of output.

The netlists are in my bsrc, filenames are tbr_euterpe-pass1.*

Tim

.

From: Jay Tomlinson [woody@ares]
Sent: Monday, September 26, 1994 11:42 AM
To: 'tbe@MicroUnity.com'
Cc: 'dane@ares'; 'graham@ares'; 'arya@ares'; 'bfox@ares'; 'wayne@ares'; 'tbr@ares'; 'albers@ares'; 'ras@ares'; 'yves@ares'; 'rich@ares'; 'pmayer@ares'; 'hestia@ares'
Subject: 9/23 pcb meeting actions

tbe@MicroUnity.com wrote (on Fri Sep 23):

Following are actions and status resulting from the pcb meeting held 9/23/94:

1) The prt files for Calliope and Euterpe do not include the giant ground pad connecting the space transformer to the pcb.

action: Jay to revise gyg files to show connection to ground.

Done. morpheus/verilog/slibsrc BOM 23.0

hestia/verilog/p620_00001_0000/BOM 38.0.

Jay

.

From: tbr
Sent: Monday, September 26, 1994 2:31 PM
To: 'Fred Obermeier'
Cc: 'dickson@aphrodite'; 'fwo@pelagon'; 'vo@aphrodite'
Subject: Re: missing csyne error
Follow Up Flag: Follow up
Flag Status: Red

Fred Obermeier wrote (on Mon Sep 26):

Tim Robinson said:
> ... no csyn message about mixed 0p, 1p, and mp inputs.

Csyn should complain about having one net drive 0p and 1p inputs.
Is there a spice deck I could look at?

Yes.

~tbr/euterpe/verilog/bsrc/tbr_euterpe-pass1.splvs

Tim

.

From: tbr
Sent: Monday, September 26, 1994 4:27 PM
To: 'doi'
Subject: stupidity
Follow Up Flag: Follow up
Flag Status: Red

OK, here's what I did. Edited the file I intended to edit. Did a checkin in a different directory which actually did nothing, but I didn't notice:

```
tbr@aphrodite ~/euterpe/verilog/bsrc/rg 450 % cd ../io
tbr@aphrodite ~/euterpe/verilog/bsrc/io 451 % cvs ci -m 'run both sections even when first one fails timing' .checkoutrc
tbr@aphrodite ~/euterpe/verilog/bsrc/io 452 % cd ../cp
tbr@aphrodite ~/euterpe/verilog/bsrc/cp 453 % cvs -n update
```

Then did the releasbom in the right place, which of course also did nothing!

Tim

From: Herman Chu [hchu@phobos.microunity.com]
Sent: Monday, September 26, 1994 6:14 PM
To: 'noel@phobos.microunity.com'; 'trancy@phobos.microunity.com'
Cc: 'hestia@phobos.microunity.com'; 'euterpe@phobos.microunity.com';
'calliope@phobos.microunity.com'; 'hchu@phobos.microunity.com'
Subject: TAB Lead Steady-state Thermal Testing/Analysis Update

In the last email I reported the estimated lead temperature for 1 lead powered on and 5 leads powered on test cases. I have completed testing on 32 leads powered on case since then. Same test conditions as before with 330 mAmps to each lead. Based upon the test results, The lead temperature is estimated to be 85 deg C at 25 deg C ambient for this case. This shows that the lead temperature will exceed 100 deg C at the worst environmental condition of 50 deg C ambient.

Trancy and I discussed these results with Geert last Friday. In his opinion, the current will be well distributed between all the power leads, therefore this scenario, where most of the current will be carried by the 62 power leads concentrated in 2 opposite corners of the Eu TAB frame, will never occur. If the current will be carried evenly among all the power leads, then each lead will only be carrying about 177 mAmps instead of the 330 mAmps, thus I don't see any thermal issue with that.

As for Calliope, there are less power leads on Calliope than Euterpe (55 leads). Similarly, if all the current is evenly distributed among them, then each lead will have about 303 mAmps. Calliope has 20 power leads concentrated at the middle portion on one side of the TAB frame. The extrapolated lead temperature is around 95 deg C at 50 deg C ambient.

In conclusion, if the current will be carried evenly among the power leads, then thermally the TAB frame should not be a problem, but Calliope's power leads are expected to be hotter than Euterpe's.

Please let me know if you guys have any questions.

Regards,
Herman

From: Alan Corry [agc@luckboy]
Sent: Monday, September 26, 1994 8:09 PM
To: 'Geert Rosseel'
Subject: nb

I am running NB in my area :

~agc/euterpe/verilog/bsrc/nb

the file "errors" is the log for this run

From: Buffalo Chip [chip@rhodan]
Sent: Monday, September 26, 1994 9:49 PM
To: 'geert@rhodan'
Subject: output of euterpe/verilog/bsrc/ctio/.checkoutrc

The output from euterpe/verilog/bsrc/ctio/.checkoutrc is 280k, so it is not included in this mail message. Instead, check the file

/n/tmp/chiplog/geert.rhodan.14108.euterpe-verilog-bsrc-ctio

(which is accessible from all machines). This file will disappear in about 5 days.

By the way, the exit status returned by .checkoutrc was 0.

From: Buffalo Chip [chip@rhea]
Sent: Monday, September 26, 1994 9:50 PM
To: 'geert@rhea'
Subject: pager log message

page from chip to geert:

Release euterpe/verilog/bsrc/ctio BOM 13.0 initiated by geert completed @ Mon Sep 26
19:48:58 PDT 1994 with exit status 0.. chip

From: Buffalo Chip [chip@rhodan]
Sent: Monday, September 26, 1994 10:17 PM
To: 'geert@rhodan'
Subject: output of euterpe/verilog/bsrc/cj/.checkoutrc

The output from euterpe/verilog/bsrc/cj/.checkoutrc is 144k, so it is not included in this mail message. Instead, check the file

/n/tmp/chiplog/geert.rhodan.18036.euterpe-verilog-bsrc-cj

(which is accessible from all machines). This file will disappear in about 5 days.

By the way, the exit status returned by .checkoutrc was 0.

From: Buffalo Chip [chip@rhea]
Sent: Monday, September 26, 1994 10:18 PM
To: 'geert@rhea'
Subject: pager log message

page from chip to geert:

Release euterpe/verilog/bsrc/cj BOM 53.0 initiated by geert completed @ Mon Sep 26
20:16:38 PDT 1994 with exit status 0.. chip

From: Geert Rosseel [geert@rhea]
Sent: Monday, September 26, 1994 11:12 PM
To: 'geert@rhea'
Subject: pager log, sender copy

page from geert to geert:

pageme gmake geert_euterpegards start:Sep_26_21:09 end: Sep_26_21:10 exit

1

From: Geert Rosseel [geert@rhea]
Sent: Monday, September 26, 1994 11:20 PM
To: 'geert@rhea'
Subject: pager log message

page from geert to geert:
pageme gmake geert_euterpegards start:Sep_26_21:12 end: Sep_26_21:18 exit
1

From: Geert Rosseel [geert@rhea]
Sent: Monday, September 26, 1994 11:21 PM
To: 'geert@rhea'
Subject: pager log, sender copy

page from geert to geert:
pageme gmake geert_euterpegards start:Sep_26_21:19 end: Sep_26_21:20 exit
1

.

From: tbr
Sent: Monday, September 26, 1994 11:22 PM
To: 'Richard Dickson'
Subject: gards check-in
Follow Up Flag: Follow up
Flag Status: Red

Richard Dickson wrote (on Mon Sep 26):

tim,

when i finish a route of a block do i 'cvs ci gards'
to get the route checked in ???

you need to copy over and add two files (if they are not there
already) then do a releasbom. You need a '.checkoutrc' and a
'clean-request'

try doing:

```
cp /u/chip/euterpe/verilog/bsrc/cdio/.checkoutrc .  
cp /u/chip/euterpe/verilog/bsrc/cdio/clean-request .  
cvs add .checkoutrc clean-request  
cvs ci -m 'your message'  
releasbom -p -m 'another message'
```

(-p means you get paged when its done).

Tim

From: Buffalo Chip [chip@staypuft]
Sent: Monday, September 26, 1994 11:34 PM
To: 'geert@staypuft'
Subject: output of euterpe/verilog/bsrc/cp/.checkoutrc

The output from euterpe/verilog/bsrc/cp/.checkoutrc is 144k, so it is not included in this mail message. Instead, check the file

/n/tmp/chiplog/geert.staypuft.1961.euterpe-verilog-bsrc-cp

(which is accessible from all machines). This file will disappear in about 5 days.

By the way, the exit status returned by .checkoutrc was 0.

.

From: Richard Dickson [dickson@demeter]
Sent: Monday, September 26, 1994 11:35 PM
To: 'tbr@demeter'
Subject: gf

tim,
i followed your recipe for gf and at the releasebom step i get this

Releasing BOM in /n/rama/s5/dickson/euterpe/verilog/bsrc/gf
mkbom: The following is found in the repository (and the most recent BOM), but not locally:
mkbom:
mkbom: Files : clean-request
mkbom:
mkbom: Error: Local directory is out-of-date with respect to the repository.
Problems with mkbom - return code 1

????? dickson

.

From: tbr
Sent: Monday, September 26, 1994 11:42 PM
To: 'Richard Dickson'
Subject: gf
Follow Up Flag: Follow up
Flag Status: Red

Richard Dickson wrote (on Mon Sep 26):

tim,
i followed your recipe for gf and at the releasebom step i get this

Releasing BOM in /n/rama/s5/dickson/euterpe/verilog/bsrc/gf
mkbom: The following is found in the repository (and the most recent BOM), but not locally:
mkbom:
mkbom: Files : clean-request
mkbom:
mkbom: Error: Local directory is out-of-date with respect to the repository.
Problems with mkbom - return code 1

????? dickson

Do a cvs update to pick up that file. Someone else already added it.
Then do the release again.

Tim

From: Buffalo Chip [chip@rhodan]
Sent: Tuesday, September 27, 1994 12:10 AM
To: 'geert@rhodan'
Subject: output of euterpe/verilog/bsrc/iq/.checkoutrc

The output from euterpe/verilog/bsrc/iq/.checkoutrc is 200k, so it is not included in this mail message. Instead, check the file

/n/tmp/chiplog/geert.rhodan.20920.euterpe-verilog-bsrc-iq

(which is accessible from all machines). This file will disappear in about 5 days.

By the way, the exit status returned by .checkoutrc was 1.

.

From: tbr
Sent: Tuesday, September 27, 1994 12:16 AM
To: 'Richard Dickson'
Subject: release on demeter
Follow Up Flag: Follow up
Flag Status: Red

Richard Dickson wrote (on Mon Sep 26):

tim,

i cant kill the job. (uchip is owner)

say 'chipq' which will display something like:

tbr@gamorra ~/euterpe/verilog/bsrc/io 407 % chipq

ID	Target Directory	Machine(pid)	Who	Stat
1	650 euterpe/verilog/bsrc/iq	rhodan(20528)	geert	1:09
2	652 euterpe/verilog/bsrc/io	gamorra(1702)	tbr	0:22
3	653 euterpe/verilog/bsrc/mc	demeter(1425)	dickson	0:09
4	654 euterpe/verilog/bsrc/gf	demeter(1766)	dickson	wait

look for the ID, (653 and 654) then you can do

chipq -k 653

chipq -k 654

which will kill them. Then on your favorite sparc 10 do

releasebom -F

in each of the appropriate directories. (The -f is needed because you have to force it to re-release an unchechged BOM). Normally only one build is allowed to run on a machine at once, so if you release them both on the same machine they will be serialized.

Let me know if you have any trouble and I'll fix it.

Tim

.

From: tbr
Sent: Tuesday, September 27, 1994 12:19 AM
To: 'ericm'
Subject: xmeter
Follow Up Flag: Follow up
Flag Status: Red

tbr@gamorra ~/euterpe/verilog/bsrc/io 412 % rsh ghidra xmeter
Error: Can't Open display
tbr@gamorra ~/euterpe/verilog/bsrc/io 413 % printenv DISPLAY
192.216.207.9:0.0

.

From: tbr
Sent: Tuesday, September 27, 1994 12:45 AM
To: 'ericm'
Subject: xmeter
Follow Up Flag: Follow up
Flag Status: Red

I figured out how to get it to run, for a few seconds at least, then:

```
tbr@godzilla ~/euterpe/verilog/bsrc/rg/gards 410 % xmeter -obd red -obg blue -o fg green godzilla trex
X Error of failed request: BadGC (invalid GC parameter)
Major opcode of failed request: 56 (X_ChangeGC)
Minor opcode of failed request: 0
Resource id in failed request: 0x14
Serial number of failed request: 106
Current serial number in output stream: 109
```

With the above command it seems to be reproducible

Tim

From: Buffalo Chip [chip@staypuft]
Sent: Tuesday, September 27, 1994 1:15 AM
To: 'geert@staypuft'
Subject: output of euterpe/verilog/bsrc/iq/.checkoutrc

Mon Sep 26 23:13:50 PDT 1994 (geert Mon, 26 Sep 1994 23:08:28 -0700)
euterpe/verilog/bsrc/iq
[Release BOM (V29.0) in euterpe/verilog/bsrc/iq (Mon Sep 26 23:13:50 PDT 1994)]

Dir euterpe/verilog/bsrc/iq BOM 29.0

22.2 .checkoutrc
12.1 1.ut
1.27 Makefile
24.4 clean-request
20.3 genpim.pl
1.17 iq.V
20.5 iq_control.pim
(20.4)
2.6 iqbr.tst
1.9 iqfree.tst
1.8 iqfree5.tst
1.8 iqhold.tst
1.9 iqhold5.tst
1.1 iqholdq2.Veqn
1.1 iqholdq7.Veqn
1.2 iqholdq9.Veqn
2.2 iqhxnumi4.Veqn
3.1 iqpredq4.Veqn
3.1 iqpredq9.Veqn
9.2 iqrst.tst
1.1 iqtrgtqs.Veqn
2.1 iqvldqt5.Veqn
20.1 pimlib.pl
20.2 power.tab.local

==> running euterpe/verilog/bsrc/iq/.checkoutrc (Mon Sep 26 23:13:56 PDT 1994) <==

gmake: `clean' is up to date.

gmake[1]: *** [gards/iq-iter] Error 1

gmake: *** [iqgards] Error 1

#

turn off pgroute

#

[-f gards/nopgroute] || touch gards/nopgroute # use padtiles # [-f gards/usepadtiles] || touch gards/usepadtiles # use pifpack # [-f gards/usepifpack] || touch gards/usepifpack # insert an instance of the clock tree # [-f gards/addclock] || touch gards/addclock # disable old dcell placement obstruction # [-f gards/noobs] || touch gards/noobs # now do it . . .

#

gmake GARDS_DISPLAY=clio:0.0 gards/iq-iter

gmake[1]: Entering directory

~/N/auspex/root/s10/chip/euterpe/verilog/bsrc/iq'

#

Final report

Done if no timing errors

Iterate if only correctable timing errors

Give up if uncorrectable timing errors

#

cp gards/ordered.all.nets gards/iq.ordered.all.nets CHIPROOT=/n/auspex/s10/chip/euterpe

/n/auspex/s10/chip/euterpe/tools/bin/topt -p

/n/auspex/s10/chip/euterpe/proteus/misc/power.tab -p gards/iq.power.tab.local \

-h /n/auspex/s10/chip/euterpe/proteus/leafgen/dclload/dclload.lib -h

/n/auspex/s10/chip/euterpe/proteus/exlax/dclload/dclload.lib -h

/n/auspex/s10/chip/euterpe/proteus/custom/dclload/dclload.lib \

```

-g /n/auspex/s10/chip/euterpe/proteus/leafgen/toptList -g
/n/auspex/s10/chip/euterpe/proteus/exlax/toptList -g
/n/auspex/s10/chip/euterpe/proteus/custom/toptList \
-A /n/auspex/s10/chip/euterpe/proteus/leafgen/caps/cap.lib -A
/n/auspex/s10/chip/euterpe/proteus/exlax/caps/cap.lib -A
/n/auspex/s10/chip/euterpe/proteus/custom/caps/cap.lib \
-H /n/auspex/s10/chip/euterpe/proteus/leafgen/time/tim.lib -H
/n/auspex/s10/chip/euterpe/proteus/custom/time/tim.lib -H
/n/auspex/s10/chip/euterpe/proteus/exlax/time/tim.lib \
-l 926 \
-e gards/iq.edif \
-K iq-base.strength \
-L iq-base.netcap \
-s gards/iq-final.stat \
-O gards/iq-final.topt.log \
-z 2 -M mobimos -R -t 50 -b 10 -a 24 -S; \ case $? in \
0) echo -n '**** converged in 0 iteration'; \
  if (expr 0 = 1 > /dev/null) then \
    echo ' ****'; \
  else \
    echo 's ****'; \
  fi; \
  touch gards/iq-iter;; \
1) if (expr 0 \> 8 > /dev/null) then \
  exit 1; \
  else \
  cp iq-base.pim gards/iq-iter.pim; \
  gmake GARDS_DISPLAY=clio:0.0 CYCLETIME=895 gards/iq-iter.garout.lis || exit 1;
\
  cp gards/iq-iter.netcap iq-base.netcap; \
  cp gards/iq-iter.strength iq-base.strength; \
  gmake GARDS_DISPLAY=clio:0.0 ITERATION=`expr 0 + 1` gards/iq-iter; \
  fi ;; \
*) exit 1;; \
esac

```

Running topt (Power OPTimizer) compiled on Tue Sep 27 00:52:10 GMT 1994

```

Processing a: Mobimos, Flop/Latch design
Consuming edif file gards/iq.edif
Found edif structure: gards_47_iq_46_edif
Flattening edif;
IQ already flat.
found 1745 instances; found 3951 nets in gards_47_iq_46_edif
Consuming power table information file
/n/auspex/s10/chip/euterpe/proteus/misc/power.tab
Consuming power table information file gards/iq.power.tab.local
Reading Stats file
/n/auspex/s10/chip/euterpe/proteus/leafgen/stats.ec1
Reading Stats file
/n/auspex/s10/chip/euterpe/proteus/leafgen/stats.cmos
Reading Stats file /n/auspex/s10/chip/euterpe/proteus/exlax/stats.ea
Reading Stats file
/n/auspex/s10/chip/euterpe/proteus/custom/stats.ec1
Reading Legal Cell List file
/n/auspex/s10/chip/euterpe/proteus/leafgen/toptList
Reading Legal Cell List file
/n/auspex/s10/chip/euterpe/proteus/exlax/toptList
Reading Legal Cell List file
/n/auspex/s10/chip/euterpe/proteus/custom/toptList
Performing Edif Transformations...
Reading DC Loads file
/n/auspex/s10/chip/euterpe/proteus/leafgen/dclload/dclload.lib
Reading DC Loads file
/n/auspex/s10/chip/euterpe/proteus/exlax/dclload/dclload.lib
Reading DC Loads file
/n/auspex/s10/chip/euterpe/proteus/custom/dclload/dclload.lib
Reading LPE extracted data from iq-base.netcap.

```

```

Reading pin cap values from
/n/auspex/s10/chip/euterpe/proteus/leafgen/caps/cap.lib
Reading pin cap values from
/n/auspex/s10/chip/euterpe/proteus/exlax/caps/cap.lib
Reading pin cap values from
/n/auspex/s10/chip/euterpe/proteus/custom/caps/cap.lib
Status information in gards/ig-final.stat Warning! Cell cgclockbias not on legal cell
list.
Any gate in it's path is not AC power optimized
No swing calculations will be performed
Pruning flattened network of unused instances... 0 pruned in 1
pass.
Checking/Setting swing values...

Reading Cap/Delay table file
/n/auspex/s10/chip/euterpe/proteus/leafgen/time/tim.lib
Reading Cap/Delay table file
/n/auspex/s10/chip/euterpe/proteus/custom/time/tim.lib
Warning! Cell cache at line 4 is not in legal cell list Warning! Cell cahalf at line 10
is not in legal cell list Warning! Cell cr at line 13 is not in legal cell list Warning!
Cell ctg at line 20 is not in legal cell list Warning! Cell gt1b at line 23 is not in
legal cell list Warning! Cell scggbfr0 at line 52 is not in legal cell list Warning!
Cell sccgdr at line 94 is not in legal cell list
Reading Cap/Delay table file
/n/auspex/s10/chip/euterpe/proteus/exlax/time/tim.lib

Connecting floating differential inputs to net vref_0ph...
Connected 0 inputs to net vref_0ph...
Reading the drive strength file Ig-base.strength and setting power levels NOTE! Cell
cgclockbias has strength of 0
DC Load checks only for cell(s):
eawwlvref56s7x4a eawwlvref20s10x1a eawwlvref16s2x4a xbc01df32s
xbc01df24s xbc01df16s xbc01df12s xbc01df8s xbc01df6s xbc01df4s
xbc01df2s xbc01 xbcmos2ecldf16s xbcmos2ecldf12s xbcmos2ecldf8s
xbcmos2ecldf4s xbcmos2ecldf2s xbcmos2ec1 Warning! No CKFI_AD1PH pin capacitance
data for cgclockbias Warning! No CKFI_BD1PH pin capacitance data for cgclockbias Warning!
No CKRI_AD1PH pin capacitance data for cgclockbias Warning! No CKRI_BD1PH pin capacitance
data for cgclockbias Warning! No CLR_ABM<8> pin capacitance data for cgclockbias Warning!
No CLR_ABM<7> pin capacitance data for cgclockbias Warning! No CLR_ABM<6> pin capacitance
data for cgclockbias Warning! No CLR_ABM<5> pin capacitance data for cgclockbias Warning!
No CLR_ABM<4> pin capacitance data for cgclockbias Warning! No CLR_ABM<3> pin capacitance
data for cgclockbias Warning! No CLR_ABM<2> pin capacitance data for cgclockbias Warning!
No CLR_ABM<1> pin capacitance data for cgclockbias Warning! No CLR_ABM<0> pin capacitance
data for cgclockbias Warning! No PHI_ANM<8> pin capacitance data for cgclockbias Warning!
No PHI_ANM<7> pin capacitance data for cgclockbias Warning! No PHI_ANM<6> pin capacitance
data for cgclockbias Warning! No PHI_ANM<5> pin capacitance data for cgclockbias Warning!
No PHI_ANM<4> pin capacitance data for cgclockbias Warning! No PHI_ANM<3> pin capacitance
data for cgclockbias Warning! No PHI_ANM<2> pin capacitance data for cgclockbias Warning!
No PHI_ANM<1> pin capacitance data for cgclockbias Warning! No PHI_ANM<0> pin capacitance
data for cgclockbias Warning! No PHI_BNM<8> pin capacitance data for cgclockbias Warning!
No PHI_BNM<7> pin capacitance data for cgclockbias Warning! No PHI_BNM<6> pin capacitance
data for cgclockbias Warning! No PHI_BNM<5> pin capacitance data for cgclockbias Warning!
No PHI_BNM<4> pin capacitance data for cgclockbias Warning! No PHI_BNM<3> pin capacitance
data for cgclockbias Warning! No PHI_BNM<2> pin capacitance data for cgclockbias Warning!
No PHI_BNM<1> pin capacitance data for cgclockbias Warning! No PHI_BNM<0> pin capacitance
data for cgclockbias Warning! No RD_BM<8> pin capacitance data for cgclockbias Warning!
No RD_BM<7> pin capacitance data for cgclockbias Warning! No RD_BM<6> pin capacitance
data for cgclockbias Warning! No RD_BM<5> pin capacitance data for cgclockbias Warning!
No RD_BM<4> pin capacitance data for cgclockbias Warning! No RD_BM<3> pin capacitance
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No RD_BM<1> pin capacitance data for cgclockbias Warning! No RD_BM<0> pin capacitance
data for cgclockbias Warning! No SI_AM<8> pin capacitance data for cgclockbias Warning!
No SI_AM<7> pin capacitance data for cgclockbias Warning! No SI_AM<6> pin capacitance
data for cgclockbias Warning! No SI_AM<5> pin capacitance data for cgclockbias Warning!
No SI_AM<4> pin capacitance data for cgclockbias Warning! No SI_AM<3> pin capacitance
data for cgclockbias Warning! No SI_AM<2> pin capacitance data for cgclockbias Warning!
No SI_AM<1> pin capacitance data for cgclockbias Warning! No SI_AM<0> pin capacitance

```


data for cgclockbias Warning! No VFFMAX pin capacitance data for cgclockbias Warning! No VFFMIN pin capacitance data for cgclockbias Warning! No VFFNOM pin capacitance data for cgclockbias Warning! No VFFREFMAX pin capacitance data for cgclockbias Warning! No VFFREFMIN pin capacitance data for cgclockbias Warning! No VFFREFNOM pin capacitance data for cgclockbias Warning! No VFFREFVAR pin capacitance data for cgclockbias Warning! No VFFVAR pin capacitance data for cgclockbias Warning! No VRRG<2> pin capacitance data for cgclockbias Warning! No VRRG<1> pin capacitance data for cgclockbias Warning! No VRRG<0> pin capacitance data for cgclockbias Warning! No XFER_BM<8> pin capacitance data for cgclockbias Warning! No XFER_BM<7> pin capacitance data for cgclockbias Warning! No XFER_BM<6> pin capacitance data for cgclockbias Warning! No XFER_BM<5> pin capacitance data for cgclockbias Warning! No XFER_BM<4> pin capacitance data for cgclockbias Warning! No XFER_BM<3> pin capacitance data for cgclockbias Warning! No XFER_BM<2> pin capacitance data for cgclockbias Warning! No XFER_BM<1> pin capacitance data for cgclockbias Warning! No XFER_BM<0> pin capacitance data for cgclockbias

Ignoring these nets:

phi_B2P phi_A2P vref_0ph

Optimizing power...

Iteration: 1

Path power optimizer

ERROR! 29 paths exceeded cycle time. Check status file.

DC Load Calculations

Unpowered Instance check: 1 found.

Savings by squeezing out extra time = (6542 - 6542) = 0.00% Change from original input
power = (6542 - 6542) = 0.00%

NOTE: 3687 unpowered nets.

Atoms:	count	atom	bjt	isrc	pld	clock
BJT Totals:	1745	10151	22446	11697	17766	8350

Memory usage: 27.750MB

Exit code: 2 (Failed Max Timing)

gmake[1]: Leaving directory

~/N/auspex/root/s10/chip/euterpe/verilog/bsrc/iq'

[finished at Mon Sep 26 23:15:27 PDT 1994 -- exit status 1]

.

From: tbr
Sent: Tuesday, September 27, 1994 1:40 AM
To: 'ericm'
Subject: xmeter
Follow Up Flag: Follow up
Flag Status: Red

OK, this time it had the decency to core dump:

```
tbr@godzilla ~/euterpe/verilog/bsrc/io 452 % xmeter -geometry +140+0 -rows 1 -w 90 -h 60 tre
x staypuft medusa cyclops tomato rhodan gamorra mothra ghidra godzilla nosferatu aphrodite -
obg 'dark slate grey' -ofg 'lime green'
Bus error (core dumped)
tbr@godzilla ~/euterpe/verilog/bsrc/io 453 % cname
xmeter
```

.

From: tbr
Sent: Tuesday, September 27, 1994 2:26 AM
To: 'doi'
Subject: Attic problem
Follow Up Flag: Follow up
Flag Status: Red

I need to put back euterpe/verilog/bsrc/io/power.tab.local (or at least put in a new version), but there is one in the Attic and no amount of cvs updates or get bombs seems to allow me to add or check in the new version. Can you fix it please?

Tim

From: Buffalo Chip [chip@rhodan]
Sent: Tuesday, September 27, 1994 2:59 AM
To: 'geert@rhodan'
Subject: output of euterpe/verilog/bsrc/cp/.checkoutrc

The output from euterpe/verilog/bsrc/cp/.checkoutrc is 120k, so it is not included in this mail message. Instead, check the file

/n/tmp/chiplog/geert.rhodan.8312.euterpe-verilog-bsrc-cp

(which is accessible from all machines). This file will disappear in about 5 days.

By the way, the exit status returned by .checkoutrc was 0.

From: Buffalo Chip [chip@rhodan]
Sent: Tuesday, September 27, 1994 3:26 AM
To: 'geert@rhodan'
Subject: output of euterpe/verilog/bsrc/cj/.checkoutrc

The output from euterpe/verilog/bsrc/cj/.checkoutrc is 120k, so it is not included in this mail message. Instead, check the file

/n/tmp/chiplog/geert.rhodan.10046.euterpe-verilog-bsrc-cj

(which is accessible from all machines). This file will disappear in about 5 days.

By the way, the exit status returned by .checkoutrc was 0.

.

From: Derek Iverson [doi@demeter]
Sent: Tuesday, September 27, 1994 10:11 AM
To: 'Tim B. Robinson'
Subject: Attic problem

Tim B. Robinson writes:

>
> I need to put back euterpe/verilog/bsrc/io/power.tab.local (or at
> least put in a new version), but there is one in the Attic and no
> amount of cvs updates or get boms seems to allow me to add or check in
> the new version. Can you fix it please?

Sure. For the future, the proper magic is:

(assuming we are in the euterpe/verilog/bsrc/io directory)

```
cvsutil unremove power.tab.local  
cvs update power.tab.local
```

I have done the 'unremove' for you. Just do an update to get the file.

doi

.

From: tbr
Sent: Tuesday, September 27, 1994 10:48 AM
To: 'Derek Iverson'
Subject: Attic problem
Follow Up Flag: Follow up
Flag Status: Red

Derek Iverson wrote (on Tue Sep 27):

Tim B. Robinson writes:

>
> I need to put back euterpe/verilog/bsrc/io/power.tab.local (or at
> least put in a new version), but there is one in the Attic and no
> amount of cvs updates or get boms seems to allow me to add or check in
> the new version. Can you fix it please?

Sure. For the future, the proper magic is:

(assuming we are in the euterpe/verilog/bsrc/io directory)

```
cvsutil unremove power.tab.local  
cvs update power.tab.local
```

I have done the 'unremove' for you. Just do an update to get the file.

Great. I'll remember that one.

Tim

From: Alan Corry [agc@luckboy]
Sent: Tuesday, September 27, 1994 11:16 AM
To: 'Geert Rosseel'
Subject: output of euterpe/verilog/bsrc/nb/.checkoutrc (fwd)

I managed to get NB to run this morning, it doesn't iterate yet.

The problem last night was that the PLAs rebuilt differently and there was a cell that didn't place.

Forwarded message:

> From chip@godzilla Tue Sep 27 09:08:32 1994
> Date: Tue, 27 Sep 94 09:08:29 PDT
> From: chip@godzilla (Buffalo Chip)
> Message-Id: <9409271608.AA09902@godzilla>
> To: agc@godzilla
> Subject: output of euterpe/verilog/bsrc/nb/.checkoutrc
>
> The output from euterpe/verilog/bsrc/nb/.checkoutrc is 176k, so it is
not included
> in this mail message. Instead, check the file
>
> /n/tmp/chiplog/agc.godzilla.5981.euterpe-verilog-bsrc-nb
>
> (which is accessible from all machines). This file will disappear in
> about 5 days.
>
> By the way, the exit status returned by .checkoutrc was 1.
>

.

From: tbe@MicroUnity.com
Sent: Tuesday, September 27, 1994 2:06 PM
To: 'Patricia Mayer'
Cc: 'woody'; 'tbr'; 'albers'; 'bfox'; 'jt'
Subject: Re: part update

On September 27, Pattie Mayer wrote:

>prt NEWS!
>
>Dan created a local library for me to deal with (Yea!) and here is the news:
>
>100_00001-Caliopie - added 12.5m ground pad (#313) to top side of board.
>
>100_00001-Euterpe - added 12.5m ground pad (#313) to top side of board.
>

Don't forget to either use the 10 mil drill vias inside this 12.5 mil square for connection to the inner layer ground plane so that they solder plug closed (and a note on the fab drawing to that effect will be required; I'll work something up). If ground vias are used outside of the 12.5 mil square, then size as required.

>180_00004 - Reworking shape (Square)
>
>270_00006 - New footprint from Brian (Override old...Same Part Number Right?)
>

This would seem to violate the form/fit/function rule. Opinion or new p/n from jt?

>370_00004 - Tom, mount holes are 1.36 apart. Data sheet specifies 1.355
>

Close enough for me and the pcb tolerance/hole float, etc.

>370_00010 - I will review. I think we'er missing mount holes.
>
>370_00011 - reworking dimensions of part. Do you want the board slotted for
> tab mounts?
>

Yes, but I will consult with fabricator to make sure its not a killer first. Go with them for now.

>370_00020 - needs non-plated mount holes
>
>370_00022 - gmake finds a 4 pin conflict. Reviewing (Woody?)
>
>370_00024 - Reviewing (Tom and I found something...)
>
>I will also edit the special symbol file locally and will create a 20 mil via
>set.
>
>Thats my list so far, let me know if I'm missing anything, - Thanks

Will do.

Tom Eich tbe@microunity.com
MicroUnity Systems Engineering, Inc.
255 Caspian Dr. Sunnyvale, CA 94089
(408)734-8100, (408)734-8136 fax

From: Buffalo Chip [chip@ghidra]
Sent: Tuesday, September 27, 1994 2:42 PM
To: 'geert@ghidra'
Subject: output of euterpe/verilog/bsrc/iq.checkoutrc

Tue Sep 27 12:40:31 PDT 1994 (geert Tue, 27 Sep 1994 12:40:07 -0700)
euterpe/verilog/bsrc/iq
[Release BOM (V30.0) in euterpe/verilog/bsrc/iq (Tue Sep 27 12:40:31 PDT 1994)]

```
Dir          euterpe/verilog/bsrc/iq                      BOM 30.0

22.3         .checkoutrc
(22.2)
12.1         1.ut
1.27        Makefile
24.4         clean-request
20.3         genpim.pl
1.17         iq.V
20.5         iq_control.pim
2.6         iqbr.tst
1.9         iqfree.tst
1.8         iqfree5.tst
1.8         iqhold.tst
1.9         iqhold5.tst
1.1         iqholdq2.Veqn
1.1         iqholdq7.Veqn
1.2         iqholdq9.Veqn
2.2         iqhxnumi4.Veqn
3.1         iqpredq4.Veqn
3.1         iqpredq9.Veqn
9.2         iqrst.tst
1.1         iqtrgtqs.Veqn
2.1         iqvldqt5.Veqn
20.1         pimlib.pl
20.2         power.tab.local
====> running euterpe/verilog/bsrc/iq/.checkoutrc (Tue Sep 27 12:40:37 PDT
1994) <====
gmake: `clean' is up to date.
#
# turn off pgroute
#
[ -f gards/nopgroute ] || touch gards/nopgroute # # use padtiles # [ -f gards/usepadtiles
] || touch gards/usepadtiles # # use pifpack # [ -f gards/usepifpack ] || touch
gards/usepifpack # # insert an instance of the clock tree # [ -f gards/addclock ] || touch
gards/addclock # # disable old dcell placement obstruction # [ -f gards/noobs ] || touch
gards/noobs # # now do it . . .
#
gmake GARDS_DISPLAY=clio:0.0 gards/iq-iter
gmake[1]: Entering directory
~/N/auspex/root/s10/chip/euterpe/verilog/bsrc/iq'
#
# Final report
#   Done if no timing errors
#   Iterate if only correctable timing errors
#   Give up if uncorrectable timing errors
#
cp gards/ordered.all.nets gards/iq.ordered.all.nets CHIPROOT=/n/auspex/s10/chip/euterpe
/n/auspex/s10/chip/euterpe/tools/bin/topt -p
/n/auspex/s10/chip/euterpe/proteus/misc/power.tab -p gards/iq.power.tab.local \
-h /n/auspex/s10/chip/euterpe/proteus/leafgen/dclload/dclload.lib -h
/n/auspex/s10/chip/euterpe/proteus/exlax/dclload/dclload.lib -h
/n/auspex/s10/chip/euterpe/proteus/custom/dclload/dclload.lib \
-g /n/auspex/s10/chip/euterpe/proteus/leafgen/toptList -g
/n/auspex/s10/chip/euterpe/proteus/exlax/toptList -g
```

```

/n/auspex/s10/chip/euterpe/proteus/custom/toptList \
-A /n/auspex/s10/chip/euterpe/proteus/leafgen/caps/cap.lib -A
/n/auspex/s10/chip/euterpe/proteus/exlax/caps/cap.lib -A
/n/auspex/s10/chip/euterpe/proteus/custom/caps/cap.lib \
-H /n/auspex/s10/chip/euterpe/proteus/leafgen/time/tim.lib -H
/n/auspex/s10/chip/euterpe/proteus/custom/time/tim.lib -H
/n/auspex/s10/chip/euterpe/proteus/exlax/time/tim.lib \
-l 926 \
-e gards/iq.edif \
-K iq-base.strength \
-L iq-base.netcap \
-s gards/iq-final.stat \
-O gards/iq-final.topt.log \
-z 2 -M mobimos -R -t 50 -b 10 -a 24 -S; \ case $? in \
0) echo -n '**** converged in 0 iteration'; \
  if (expr 0 = 1 > /dev/null) then \
    echo ' ****'; \
  else \
    echo 's ****'; \
  fi; \
touch gards/iq-iter;; \
1) if (expr 0 \> 8 > /dev/null) then \
  exit 1; \
else \
  cp iq-base.pim gards/iq-iter.pim; \
  gmake GARDS_DISPLAY=clio:0.0 CYCLETIME=895 gards/iq-iter.garout.lis || exit 1;
\
  cp gards/iq-iter.netcap iq-base.netcap; \
  cp gards/iq-iter.strength iq-base.strength; \
  gmake GARDS_DISPLAY=clio:0.0 ITERATION=`expr 0 + 1` gards/iq-iter; \
  fi ; \
*) exit 1;; \
esac

```

Running topt (Power OPTimizer) compiled on Tue Sep 27 00:52:10 GMT 1994

```

Processing a: Mobimos, Flop/Latch design
Consuming edif file gards/iq.edif
Found edif structure: gards_47_iq_46_edif
Flattening edif;
IQ already flat.
Found 1745 instances; found 3951 nets in gards_47_iq_46_edif
Consuming power table information file
/n/auspex/s10/chip/euterpe/proteus/misc/power.tab
Consuming power table information file gards/iq.power.tab.local
Reading Stats file
/n/auspex/s10/chip/euterpe/proteus/leafgen/stats.ec1
Reading Stats file
/n/auspex/s10/chip/euterpe/proteus/leafgen/stats.cmos
Reading Stats file /n/auspex/s10/chip/euterpe/proteus/exlax/stats.ea
Reading Stats file
/n/auspex/s10/chip/euterpe/proteus/custom/stats.ec1
Reading Legal Cell List file
/n/auspex/s10/chip/euterpe/proteus/leafgen/toptList
Reading Legal Cell List file
/n/auspex/s10/chip/euterpe/proteus/exlax/toptList
Reading Legal Cell List file
/n/auspex/s10/chip/euterpe/proteus/custom/toptList
Performing Edif Transformations...
Reading DC Loads file
/n/auspex/s10/chip/euterpe/proteus/leafgen/dclload/dclload.lib
Reading DC Loads file
/n/auspex/s10/chip/euterpe/proteus/exlax/dclload/dclload.lib
Reading DC Loads file
/n/auspex/s10/chip/euterpe/proteus/custom/dclload/dclload.lib
Reading LPE extracted data from iq-base.netcap.

Reading pin cap values from

```

```

/n/auspex/s10/chip/euterpe/proteus/leafgen/caps/cap.lib
  Reading pin cap values from
/n/auspex/s10/chip/euterpe/proteus/exlax/caps/cap.lib
  Reading pin cap values from
/n/auspex/s10/chip/euterpe/proteus/custom/caps/cap.lib
  Status information in gards/iq-final.stat Warning! Cell cgclockbias not on legal cell
list.
  Any gate in it's path is not AC power optimized
  No swing calculations will be performed
  Pruning flattened network of unused instances... 0 pruned in 1
pass.
  Checking/Setting swing values...

  Reading Cap/Delay table file
/n/auspex/s10/chip/euterpe/proteus/leafgen/time/tim.lib
  Reading Cap/Delay table file
/n/auspex/s10/chip/euterpe/proteus/custom/time/tim.lib
Warning! Cell cache at line 4 is not in legal cell list Warning! Cell cahalf at line 10
is not in legal cell list Warning! Cell cr at line 13 is not in legal cell list Warning!
Cell cttag at line 20 is not in legal cell list Warning! Cell gtlb at line 23 is not in
legal cell list Warning! Cell scggbfr0 at line 52 is not in legal cell list Warning!
Cell sccgdr at line 94 is not in legal cell list
  Reading Cap/Delay table file
/n/auspex/s10/chip/euterpe/proteus/exlax/time/tim.lib

  Connecting floating differential inputs to net vref_0ph...
  Connected 0 inputs to net vref_0ph...
  Reading the drive strength file iq-base.strength and setting power levels NOTE! Cell
cgclockbias has strength of 0
  DC Load checks only for cell(s):
  eawwlvref56s7x4a eawwlvref20s10x1a eawwlvref16s2x4a xbc01df32s
  xbc01df24s xbc01df16s xbc01df12s xbc01df8s xbc01df6s xbc01df4s
  xbc01df2s xbc01 xbcmos2ecldf16s xbcmos2ecldf12s xbcmos2ecldf8s
  xbcmos2ecldf4s xbcmos2ecldf2s xbcmos2ec1 Warning! No CKFI_AD1PH pin capacitance
data for cgclockbias Warning! No CKFI_BD1PH pin capacitance data for cgclockbias Warning!
No CKRI_AD1PH pin capacitance data for cgclockbias Warning! No CKRI_BD1PH pin capacitance
data for cgclockbias Warning! No CLR_ABM<7> pin capacitance data for cgclockbias Warning!
No CLR_ABM<6> pin capacitance data for cgclockbias Warning! No CLR_ABM<5> pin capacitance
data for cgclockbias Warning! No CLR_ABM<4> pin capacitance data for cgclockbias Warning!
No CLR_ABM<3> pin capacitance data for cgclockbias Warning! No CLR_ABM<2> pin capacitance
data for cgclockbias Warning! No CLR_ABM<1> pin capacitance data for cgclockbias Warning!
No CLR_ABM<0> pin capacitance data for cgclockbias Warning! No PHI_ANM<8> pin capacitance
data for cgclockbias Warning! No PHI_ANM<7> pin capacitance data for cgclockbias Warning!
No PHI_ANM<6> pin capacitance data for cgclockbias Warning! No PHI_ANM<5> pin capacitance
data for cgclockbias Warning! No PHI_ANM<4> pin capacitance data for cgclockbias Warning!
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data for cgclockbias Warning! No PHI_ANM<1> pin capacitance data for cgclockbias Warning!
No PHI_ANM<0> pin capacitance data for cgclockbias Warning! No PHI_BNM<8> pin capacitance
data for cgclockbias Warning! No PHI_BNM<7> pin capacitance data for cgclockbias Warning!
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No SI_AM<7> pin capacitance data for cgclockbias Warning! No SI_AM<6> pin capacitance
data for cgclockbias Warning! No SI_AM<5> pin capacitance data for cgclockbias Warning!
No SI_AM<4> pin capacitance data for cgclockbias Warning! No SI_AM<3> pin capacitance
data for cgclockbias Warning! No SI_AM<2> pin capacitance data for cgclockbias Warning!
No SI_AM<1> pin capacitance data for cgclockbias Warning! No SI_AM<0> pin capacitance
data for cgclockbias Warning! No VFFMAX pin capacitance data for cgclockbias Warning! No
VFFMLN pin capacitance data for cgclockbias Warning! No VFFNOM pin capacitance data for

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cgclockbias Warning! No VFFREFMAX pin capacitance data for cgclockbias Warning! No VFFREFMIN pin capacitance data for cgclockbias Warning! No VFFREFNOM pin capacitance data for cgclockbias Warning! No VFFREFVAR pin capacitance data for cgclockbias Warning! No VFFVAR pin capacitance data for cgclockbias Warning! No VRRG<2> pin capacitance data for cgclockbias Warning! No VRRG<1> pin capacitance data for cgclockbias Warning! No VRRG<0> pin capacitance data for cgclockbias Warning! No XFER_BM<8> pin capacitance data for cgclockbias Warning! No XFER_BM<7> pin capacitance data for cgclockbias Warning! No XFER_BM<6> pin capacitance data for cgclockbias Warning! No XFER_BM<5> pin capacitance data for cgclockbias Warning! No XFER_BM<4> pin capacitance data for cgclockbias Warning! No XFER_BM<3> pin capacitance data for cgclockbias Warning! No XFER_BM<2> pin capacitance data for cgclockbias Warning! No XFER_BM<1> pin capacitance data for cgclockbias Warning! No XFER_BM<0> pin capacitance data for cgclockbias

Ignoring these nets:
phi_B2P phi_A2P vref_0ph

Optimizing power...

Iteration: 1

Path power optimizer

ERROR! 29 paths exceeded cycle time. Check status file.

DC Load Calculations

Unpowered Instance check: 1 found.

Savings by squeezing out extra time = (6542 - 6542) = 0.00% Change from original input
power = (6542 - 6542) = 0.00%

NOTE: 3687 unpowered nets.

Atoms:	count	atom	bjt	isrc	pld	clock
BJT Totals:	1745	10151	22446	11697	17766	8350

Memory usage: 27.750MB

Exit code: 2 (Failed Max Timing)

gmake[1]: *** [gards/iq-iter] Error 1

gmake[1]: Leaving directory

~/N/auspex/root/s10/chip/euterpe/verilog/bsrc/iq'

gmake: *** [iqgards] Error 1

[finished at Tue Sep 27 12:42:12 PDT 1994 -- exit status 1]

From: Buffalo Chip [chip@rhodan]
Sent: Tuesday, September 27, 1994 4:02 PM
To: 'geert@rhodan'
Subject: output of euterpe/verilog/bsrc/iq/.checkoutrc

The output from euterpe/verilog/bsrc/iq/.checkoutrc is 200k, so it is not included in this mail message. Instead, check the file

/n/tmp/chiplog/geert.rhodan.28063.euterpe-verilog-bsrc-iq

(which is accessible from all machines). This file will disappear in about 5 days.

By the way, the exit status returned by .checkoutrc was 1.

.

From: Eric Murray [ericm@MicroUnity.com]
Sent: Tuesday, September 27, 1994 4:14 PM
To: 'vant'
Cc: 'sysadmin@MicroUnity.com'; 'vanthof@MicroUnity.com'; 'hopper@MicroUnity.com'; 'tbr@MicroUnity.com'; 'rozen@MicroUnity.com'
Subject: Re: network funnies from medusa to ghidra?

vant wrote:

>
>
> I just had a large verification job die with this error message:
>
> /u/chip/tools/bin/sun4/vlsimm: fatal error detected by vlsi (code 0):
> can't find cell 'chunk1159_EUTERPE' (boo file '</>::/u/vanthof/compass/
> mobi/euterpe/vlsi.boo')
>
> Error detected by gridcheck (vlsimm).
>
>
> This process was running on medusa looking for a file on ghidra.
>
> The file does exist:
>
> Vant@hestia-> ls -l /n/ghidra/s5/vo/euterpe/compass/save1/chunk1159_euterpe.ly
>
> -rw-rw-r-- 1 vo 1301 Sep 24 19:06 /n/ghidra/s5/vo/euterpe/compass/save1/chunk1159_euterpe.ly
>
>
> This particular process reads this file multiple times and it was after
> about the 4th time of finding the file, that this error message occurred.
>
> I also noticed that the process load on ghidra went up to about 20 near
> that same moment in time. Would a large process load cause this sort of
> 'network timeout' to occur? And if so, how can we fix this.

it looks like that's exactly what happened.

there's some NFS parameters i can hack via amd, it would probably require
a reboot to get them to take effect.

i've put in for some equipment so i can set up a high-speed network
for the sparc10s, since y'all are cross-mounting them much more
than i anticipated. each sparc10 will have a full 10meg ethernet
connection to a dedicated router, and the router will be plugged
into the fddi backbone and also have a dedicated fddi to the auspex.

--
ericm ericm@microunity.com

.

From: Derek Iverson [doi@demeter]
Sent: Tuesday, September 27, 1994 4:29 PM
To: 'Tim B. Robinson'
Subject: getbom hung

Tim B. Robinson writes:

>

> Please look on my screen. I did a getbom and i has just hung. . .

I noticed that there was a CVS lock file in

euterpe/verilog/bsrc/ld (or whatever path it was)

with a time stamp of Sept 27 at 1:37 pm.

I punted it and the getbom continued.

doi

.

From: vant [vanthof@hestia]
Sent: Tuesday, September 27, 1994 5:01 PM
To: 'sysadmin@hestia'
Cc: 'Dave Van't Hof'; 'Mark Hofmann'; 'Tim B. Robinson'; 'Don Rozenberg'
Subject: network funnies from medusa to ghidra?

I just had a large verification job die with this error message:

```
/u/chip/tools/bin/sun4/vlsimm: fatal error detected by vlsi (code 0):  
can't find cell 'chunk1159_EUTERPE' (boo file '<./>::/u/vanthof/compass/  
mobi/euterpe/vlsi.boo')
```

Error detected by gridcheck (vlsimm).

This process was running on medusa looking for a file on ghidra.

The file does exist:

```
Vant@hestia-> ls -l /n/ghidra/s5/vo/euterpe/compass/save1/chunk1159_euterpe.ly  
-rw-rw-r-- 1 vo      1301 Sep 24 19:06 /n/ghidra/s5/vo/euterpe/compass/save1/chunk1159_euterpe.ly
```

This particular process reads this file multiple times and it was after about the 4th time of finding the file, that this error message occurred.

I also noticed that the process load on ghidra went up to about 20 near that same moment in time. Would a large process load cause this sort of 'network timeout' to occur? And if so, how can we fix this.

Unfortunately, this process is not restartable and must be rerun from the beginning (multiple hours lost).

Thanks,
Dave

--
Dave Van't Hof vanthof@microunity.com MicroUnity Systems Engineering, Inc.
"What rolls down stairs, alone or in pairs, rolls over the neighbor's dog?
What's great for a snack and fits on your back? It's log, log, log!"
LOG from BLAMMO! (tm) All kids love Log! #include <std_disclaim.h>

From: Buffalo Chip [chip@ghidra]
Sent: Tuesday, September 27, 1994 5:34 PM
To: 'geert@ghidra'
Subject: output of euterpe/verilog/bsrc/cj/.checkoutrc

The output from euterpe/verilog/bsrc/cj/.checkoutrc is 144k, so it is not included in this mail message. Instead, check the file

/n/tmp/chiplog/geert.ghidra.17035.euterpe-verilog-bsrc-cj

(which is accessible from all machines). This file will disappear in about 5 days.

By the way, the exit status returned by .checkoutrc was 0.

From: Buffalo Chip [chip@rhodan]
Sent: Tuesday, September 27, 1994 5:49 PM
To: 'geert@rhodan'
Subject: output of euterpe/verilog/bsrc/cp/.checkoutrc

The output from euterpe/verilog/bsrc/cp/.checkoutrc is 152k, so it is not included in this mail message. Instead, check the file

/n/tmp/chiplog/geert.rhodan.4976.euterpe-verilog-bsrc-cp

(which is accessible from all machines). This file will disappear in about 5 days.

By the way, the exit status returned by .checkoutrc was 0.

.

From: tbr
Sent: Tuesday, September 27, 1994 8:16 PM
To: 'Eric Murray'
Cc: 'hopper@MicroUnity.com'; 'rozen@MicroUnity.com'; 'sysadmin@MicroUnity.com'; 'vanthof@MicroUnity.com'; 'vant'
Subject: Re: network funnies from medusa to ghidra?
Follow Up Flag: Follow up
Flag Status: Red

Eric Murray wrote (on Tue Sep 27):

vant wrote:
>
>
> I just had a large verification job die with this error message:
>
> /u/chip/tools/bin/sun4/vlsimm: fatal error detected by vlsi (code 0):
> can't find cell 'chunk1159_EUTERPE' (boo file '<./>::/u/vanthof/compass/
> mobi/euterpe/vlsi.boo')
>
> Error detected by gridcheck (vlsimm).
>
>
> This process was running on medusa looking for a file on ghidra.
>
> The file does exist:
>
> Vant@hestia-> ls -l /n/ghidra/s5/vo/euterpe/compass/save1/chunk1159_euterpe.ly
>
> -rw-rw-r-- 1 vo 1301 Sep 24 19:06 /n/ghidra/s5/vo/euterpe/compass/save1/chunk1159_euterpe.ly
>
>
> This particular process reads this file multiple times and it was after
> about the 4th time of finding the file, that this error message occurred.
>
> I also noticed that the process load on ghidra went up to about 20 near
> that same moment in time. Would a large process load cause this sort of
> 'network timeout' to occur? And if so, how can we fix this.

it looks like that's exactly what happened.

there's some NFS parameters i can hack via amd, it would probably require
a reboot to get them to take effect.

i've put in for some equipment so i can set up a high-speed network
for the sparcl0s, since y'all are cross-mounting them much more
than i anticipated. each sparcl0 will have a full 10meg ethernet
connection to a dedicated router, and the router will be plugged
into the fddi backbone and also have a dedicated fddi to the auspex.

Is there any way to set up the retries to an unlimited number,
equivalent to the old 'hard mount' of before the automounter?

From: Fred Obermeier [fwo@pelagon]
Sent: Tuesday, September 27, 1994 8:17 PM
To: 'fwo@pelagon'; 'stick@pelagon'; 'vanthof@pelagon'
Cc: 'geert@pelagon'; 'tvo@pelagon'
Subject: Orchis LVS

Dave,

A vdde/vsse short was found and was caused by a mislabeled pad type in the padlist.lst. The die used a padvssvdda to bring out vsse on metal 5. However, padlist.lst had this declared as a padvdda and connected to vdde sense, a vdde signal. Therefore SM3 connected to vdde while the M5 connected to M5. This causes a vdde/vsse short.

Padlist.lst has been changed so that pad 278 is labelled as a vsse pad on the die (testram.ly) and uses a pad of type padvssvdda. Externally, this pad is still labelled vdde since it is still a vdde sense line.

I've cvs checked in this change and the releasebom has rebuilt most layout files under /u/chip/orchis/compass/baseplate/.

You should probably kill the current running LVS since it will have this short, and pick up the new version of /u/chip/orchis/compass/baseplate/ spacetrans_padring.ly and stoutvdda_padring.ly into the snapshot.

Despite this confused description, Bruce and I think we understand what when wrong.

We won't see this error for euterpe or calliope, since these parts make use of the automatically generated baseplate pad list.

Thanks,
Fred.

From: Mark Hofmann [hopper@tomato]
Sent: Wednesday, September 28, 1994 4:20 AM
To: 'sysadm@tomato'; 'Don Rozenberg'
Cc: 'vant@tomato'; 'Tim B. Robinson'
Subject: Large partitions need on Dracula machines

Hi,

In order to tapeout our next round of chips we need to have as large a single disk partition as possible. I believe this is about 2GB. Here are the way things stand currently on the 4 Dracula machines:

```
mothra/ df
Filesystem      kbytes  used  avail capacity Mounted on
/dev/sd0a       49285   6806  37551   15%  /
/dev/sd0g       342305  246276  61799   80%  /usr
/dev/sd2g       1962485  883999  882238   50%  /s2
/dev/sd3g       1962485  1726541  39696   98%  /s3
/dev/sd1g       819286   3477  733881    0%  /s4
```

```
tomato/ df
Filesystem      kbytes  used  avail capacity Mounted on
/dev/sd0a       48591   7368  36364   17%  /
/dev/sd0g       348479  101720  211912   32%  /usr
/dev/sd2g       1629014  684986  927738   42%  /s1
/dev/sd3g       1629014  1080063  532661   67%  /s2
/dev/sd3h       1042702  837665  194610   81%  /s3
```

```
cyclops/ df
Filesystem      kbytes  used  avail capacity Mounted on
/dev/sd0a       48591   8235  35497   19%  /
/dev/sd0g       348479  92698  220934   30%  /usr
/dev/sd2g       1629014  1025057  441056   70%  /s1
/dev/sd3g       1629014  514429  951684   35%  /s2
```

```
medusa/ df
Filesystem      kbytes  used  avail capacity Mounted on
/dev/sd0a       31967   7146  21625   25%  /
/dev/sd0g       870214  651734  131459   83%  /usr
/dev/sd1g       523575  144409  373931   28%  /s1
/dev/sd2g       1666773  541678  1108428   33%  /s2
/dev/sd3g       1666773    17  1650089    0%  /s3
```

Note that mothra has bigger partitions than the other 3 machines. Could we make all machines uniform in disk size (unless different disks prohibit this)? Also, let's reduce the number of blocks reserved for i-nodes. Verification jobs produce a small number of huge files, we need the disk space for the data.

-thanks,
hopper

.

From: tbr
Sent: Wednesday, September 28, 1994 11:06 AM
To: 'vant'
Cc: 'Brian Lee'; 'dickson'; 'mws'; 'billz'; 'agc'; 'woody'; 'Geert Rosseel'; 'Mark Hofmann'; 'Lisa Robinson'; 'Dave Van't Hof'; 'Tom Vo'
Subject: medusa being thrashed by chip
Follow Up Flag: Follow up
Flag Status: Red

vant wrote (on Wed Sep 28):

There's about 7 or 8 espresso jobs running on medusa which is completely thrashing the drc job running there and the system load is about 11. I've niced down a few of the jobs, but they seem to be regenerative.

Does anyone know why this is happening?

My guess is that someone has done a releasebom of euterpe/verilog/bsrc on that machine. Because hopper had released new version of the pla tools all the pla's will regenerate. The bulk of it takes only about a half hour (it intentionally uses the parallel option on make and I would expect the load to hit 12 for a short time), but there is a tail end of two prallel jobs that runs on for a couple of hours (but I would not have expected those cases to have been triggered).

Something is odd though, because lisar got a page about 6.30 am this morning to say that release was underway, yet the checkin happened at around 6pm last night.

As far as I can see what happened was that there were several builds going on in the sub sections, one of which did not complete till after 6 this morning. Becuse of the interlocks, that caused the bsrc relase to be held off.

I see you have the remaining jobs niced, and there is essentially nothing else to be done after they complete, do if they are not a problem niced (and memory use is tiny), we should leave them.

If not, they could be killed and we could force a re-release on another machine. Clearly it is a mistake for a release in bsrc to happen on one of the verification machines.

Tim

.

From: Mark Hofmann [hopper@tomato]
Sent: Wednesday, September 28, 1994 11:26 AM
To: 'Tim B. Robinson'
Cc: 'Alan Corry'
Subject: no PIFPACKing

Hi Tim,

Alan has a situation where for 3 sections of Euterpe he does not want to pifpack cells. He can get this effect by removing the "usepifpack" file, but ideally we would want to control this through use of a define in the Makefile. Did we have this set up at one time? One way to not pifpack something would be to say:

```
gmake PIFPACK_SQUEEZE=-1 PIFPACK_DISTANCE=-1 FOOGards
```

but perhaps we could make this a little more obvious with

```
USEPIFPACK=0
```

or some such.

-hopper

From: Jay Tomlinson [woody@ares]
Sent: Wednesday, September 28, 1994 11:55 AM
To: 'euterpe@ares'
Subject: Final Decision: Data Cache Tag bits 63:48 ignored by hardware.

This decision is final:

woody wrote (on Thu Sep 22):

Decision to become final at midnight on Monday 9/26/94.

The data cache tag currently consists of:

63:6 physical address of the data.
5:1 protection information
0 dirty bit.

the physical address is compared to the physical address generated by the instruction. If they match then the cache data can be used. If they do not match, then the physical address (generated by the instruction) will be used to fetch the data to be written into the cache.

Also, if physical address bits 63:48 are not all zero, then an Illegal Address exception will be reported and the cache data will not be fetched and written into the data cache. This means that the hardware will never write the tag with any of bits 63:48 non-zero as part of a cache fill. The only way that any of these bits can be written non-zero, is by SW (store directly to the data cache tag). If SW does this, then when the cache line is accessed either a cache miss will occur or an exception will be reported due to the physical address having non-zero a value in bits 63:48.

This means that bits 63:48 are essentially useless since they can never be non-zero and meaningful.

Therefore I propose that the cache tag be logically viewed as only consisting of bits 47:6 of the physical address. These bits would not be matched to the physical address and would written/read as zero.

Jay

From: vant [vanthof@hestia]
Sent: Wednesday, September 28, 1994 4:24 PM
To: 'Orlando Hernando'; 'Mike Wageman'
Cc: 'Dave Van't Hof'; 'Mark Hofmann'; 'Geert Rosseel'; 'Tom Vo'
Subject: euterpe upper drc's finished

Hi.

The euterpe upper drc's finished and it's not that bad. I have not looked at it personally, but I think it's only edge errors and offgrid pads.

It's:

/u/vanthof/compass/mobi/euterpe/euterpe_upper.err

I was wondering if either of you could look at this sometime soon?

Thanks,
Dave

--

Dave Van't Hof vanthof@microunity.com MicroUnity Systems Engineering,
Inc.

"What rolls down stairs, alone or in pairs, rolls over the neighbor's dog?"

What's great for a snack and fits on your back? It's log, log, log!"

LOG from BLAMMO! (tm) All kids love Log! #include

<std_disclaim.h>

From: Tom Vo [vo@merope]
Sent: Wednesday, September 28, 1994 5:24 PM
To: 'vant'
Cc: 'vanthof@hestia'; 'Mark Hofmann'; 'Geert Rosseel'; 'Tim B. Robinson'; 'Lisa Robinson'; 'John Campbell'; 'Fred Obermeier'; 'Haim Horovitz'
Subject: Re: euterpe upper drc's finished

I looked at the upper drc results . I think they're all false errors .

M5 offgrid error : old errors due to an overly aggressive M5 grid check If we passed this test , then we probably won't have a problem with s.t. construction . If we failed , then we may or may not have a problem with the s.t . I believe that if we build a s.t. today , we won't have a problem (excluding the PLLs -- this layout is not completed)

A bunch of errors in the seal ring / layer id / copy right area :
Things having to do with maximum width restriction , M5 w.o. V45 .

A bunch more errors from not having a s.t. .

I did not cycle through the errors one by one . I only looked at them from a distance .

tvo

.

From: vant [vanthof@hestia]
Sent: Wednesday, September 28, 1994 5:55 PM
To: 'Tom Vo'
Cc: 'hopper@merope'; 'geert@merope'; 'tbr@merope'; 'lisar@merope'; 'solo@merope'; 'fwo@merope'; 'haim@merope'
Subject: Re: euterpe upper drc's finished

Tom Vo writes:

>
>
>I looked at the upper drc results . I think they're all false errors .
>
>M5 offgrid error : old errors due to an overly aggressive M5 grid check
>If we passed this test , then we probably won't have a problem with s.t .
>construction . If we failed , then we may or may not have a problem with
>the s.t . I believe that if we build a s.t. today , we won't have a problem
>(excluding the PLLs -- this layout is not completed)

Hmm. The majority of errors are from this check. Hopefully this can be resolved. Haim should be back soon.

>
>A bunch of errors in the seal ring / layer id / copy right area :
>Things having to do with maximum width restriction , M5 w.o. V45 .

These are quite normal, although, I'm not familiar with any max width checks. These might need more investigating.

>
>A bunch more errors from not having a s.t .
>
>I did not cycle through the errors one by one . I only looked at them from
>a distance .

Thanks,
Dave

--
Dave Van't Hof vanthof@microunity.com MicroUnity Systems Engineering, Inc.
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LOG from BLAMMO! (tm) All kids love Log! #include <std_disclaim.h>

From: Guillermo A. Loyola [gmo@MicroUnity.com]
Sent: Wednesday, September 28, 1994 5:59 PM
To: 'lisa@MicroUnity.com'
Subject: Fwd fyi

From guarino@thessalus Wed Sep 28 15:56:25 1994
Received: from thessalus.microunity.com by bilbo.microunity.com via SMTP
(9311110.SGI.ANONFTP/920502.SGI)
for gmo id AA27454; Wed, 28 Sep 94 15:56:25 -0700
Received: from [127.0.0.1] by thessalus.microunity.com
(8.6.4/muse-sw.2)
id PAA04247; Wed, 28 Sep 1994 15:56:04 -0700
Message-Id: <199409282256.PAA04247@thessalus.microunity.com>
To: wayne@thessalus, doi@thessalus, jeffm@thessalus, iimura@thessalus,
gmo@thessalus, sandeep@thessalus
Cc: guarino@thessalus
Subject: today's bring-up meeting
Date: Wed, 28 Sep 94 15:56:02 -0700
From: Loretta Guarino <guarino@thessalus>

Today's meeting focused primarily on the hardware support for bring-up. We'll meet again next Wednesday, Oct. 5, at 10:30.

Action items:

Wayne:

1. confirm with Tim that there is some way to turn off the Euterpe clock, so the CBI can be the master
2. talk with Tim about whether the start vector address can be set to boot from mCerberus, instead of hardwired to boot from ROM
3. change board design for development to have a socket for the Flash ROM

Sandeep and Derek:

1. implement parallel port device drivers for sun and sgi

Jeff:

1. investigate what hardware support is needed to be able to run tests from different locations (e.g. buffer, ROM, RAM, Cerberus)
2. write up plan for external aspects of test control

Wayne and Sandeep:

1. develop a strategy so that the workstation can respond to read requests before the request times out

Jeff, Wayne, Gmo:

1. develop plans for a quick and dirty characterization test

Gmo:

1. write up a plan for virtual devices and their interaction with gdb
2. confirm with Tim which Cerberus bit will cause a Euterpe event

.

From: vant [vanthof@hestia]
Sent: Wednesday, September 28, 1994 8:21 PM
To: 'Geert Rosseel'
Cc: 'Dave Van't Hof'; 'Tim B. Robinson'; 'Mark Hofmann'
Subject: Re: more topt questions :

Geert Rosseel writes:

I believe all of the errors you reported are caused by reading in a corrupted strength file.

For instance, when I look at the geert_euterpe-iter.topt.log, there are many ERRORS that topt is spitting out:

```
*****  
                                ERROR! Instance gt/UgtSnake/UmuxCtl/Uahold_2/u0 (basename: xbor7)  
is being set to basename xbor5 from strength file at line 17588.  
    This is a very very bad thing to do!  
*****
```

This would cause the errors for missing pincaps, sdl errors, extra input pins, etc. This is a very very bad thing to have happen. Please check how the strength file is being generated.

The above error is caused when the gate type for a specific instance was changed. Ie, the strength file says that the gate is an OR5, but the edif netlist now says it's an OR7. Topt can not deal with this cleanly.

Topt sets the return code to 3 (bad input) because it is a bad input file, however, the -0 flag overrides this and will set the return code to 0. Maybe this should be changed?

Anyway, the data being fed to topt would cause all kinds of bad things to happen...

Hope this helps.
Dave

--
Dave Van't Hof vanthof@microunity.com MicroUnity Systems Engineering, Inc.
"What rolls down stairs, alone or in pairs, rolls over the neighbor's dog?
What's great for a snack and fits on your back? It's log, log, log!"
LOG from BLAMMO! (tm) All kids love Log! #include <std_disclaim.h>

.

From: Wayne Freitas [wayne@echidna]
Sent: Wednesday, September 28, 1994 8:39 PM
To: 'tbr@echidna'
Subject: Cerberus questions

Tim, I attending our on again, off again bring-up meeting with a couple of the software people and came away with pretty much the same action items that I got over 4 months ago.

Are you still planning on having Euterpe support a master/slave mode for the Cerberus Bus Interface tool.

Can we force Euterpe to fetch from the Cerberus Bus address upon reset by forcing a special register to be set.

Wayne

.

From: Haim Horovitz [haim@boreas]
Sent: Wednesday, September 28, 1994 10:44 PM
To: 'vant'
Cc: 'vo@merope'; 'hopper@merope'; 'geert@merope'; 'tbr@merope'; 'lisar@merope'; 'solo@merope';
'two@merope'; 'haim@merope'
Subject: Re: euterpe upper drc's finished

I'll look at it tomorrow morning.

Haim

> the words of vant:
==>
==>Tom Vo writes:
==>>
==>>
==>>I looked at the upper drc results . I think they're all false errors .
==>>
==>>M5 offgrid error : old errors due to an overly aggressive M5 grid check
==>>If we passed this test , then we probably won't have a problem with s.t.
==>>construction . If we failed , then we may or may not have a problem with
==>>the s.t . I believe that if we build a s.t. today , we won't have a problem
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==>
==>Hmm. The majority of errors are from this check. Hopefully this can
==>be resolved. Haim should be back soon.
==>
==>>
==>>A bunch of errors in the seal ring / layer id / copy right area :
==>>Things having to do with maximum width restriction , M5 w.o. V45 .
==>
==>>These are quite normal, although, I'm not familiar with any max width
==>>checks. These might need more investigating.
==>
==>>
==>>A bunch more errors from not having a s.t. .
==>>
==>>I did not cycle through the errors one by one . I only looked at them from
==>>a distance .
==>
==>Thanks,
==>Dave
==>
==>..
==>>Dave Van't Hof vanthof@microunity.com MicroUnity Systems Engineering, Inc.
==>>"What rolls down stairs, alone or in pairs, rolls over the neighbor's dog?
==>>What's great for a snack and fits on your back? It's log, log, log!"
==>>LOG from BLAMMO! (tm) All kids love Log! #incluce <std_disclaim.h>
==>

--
Haim Horovitz haim@microunity.com
MicroUnity Systems Engineering, Inc.
255 Caspian Way, Sunnyvale, CA 94089

Tel: (408) 734-8100 X332

From: Lisa Robinson [lisar@nosferatu]
Sent: Wednesday, September 28, 1994 11:46 PM
To: 'staffers@nosferatu'; 'jt@nosferatu'; 'hopper@nosferatu'
Subject: Schedule meeting action items.

Action items from today's schedule meeting.

tbr Needs to get with Craig this afternoon to finailize the event daemon architecture.

steve To provide mouss with the details of the PCB contract/placement agreement with a view to working with them re. hopper's position opening.

hopper Into final Euterpe verification so will require round the clock sysadm support.

mouss To pass graham a resume re. wireless position opening.

graham Channel 3/4 modulation is at least 10% of the available machine cycles. Is this the right way to go? Graham to call meeting.

graham/curtis ISDN product realization should be planned for. Curtis may need more headcount. Should plan for shipment of 30,000 ISDN mediacomputers during the first 6 months of next year.

lisar Needs a technician to support wayne. lisar will go ahead with pursuing filling this position.

lisar Requires design groups to adhere to the board/box bringup plan jointly developed with the design groups. Plan calls for test result documentation and problem tracking where appropriate. lisar should be more avidly selling the approach. graham requested a meeting to go over the test plan details.

mudge lisar thinks johnny needs something (test vectors?) from her group for calliope test. Johnny and lisar should get together.

Al I got the impression that the test wafer discussion was a non-issue but just to clarify. The castor/pollux and orchis masks will be processed in parallel in the fab. Castor/pollux will be used to debug the process and orchis will be used as a yield monitor once we have yielding castor/pollux transistors. Al to clarify.

lisar JT would like to have a streamlined process for producing/approving the documentation associated with fabrication of box parts. Lisar to look into automating this.

steve Should buy for the build of 50 units on 10/31.

curtis Needs to look at improving NTSC performance.

Van Dyke Needs the Mayan license agreement

Van Dyke Needs a stable NT machine. Someone (?) should get a configuration from Seattle.

Lisa R.

From: vant [vanthof@hestia]
Sent: Thursday, September 29, 1994 8:22 AM
To: 'Richard Dickson'
Cc: 'cadettes@hestia'; 'Dave Van't Hof'; 'Geert Rossee!'
Subject: Re: gmake guards

Richard Dickson writes:

```
>
>you'all,
>
>    both of my guards just failed. i get this in my log file.
>
>CHIPROOT=/n/rama/s5/dickson/euterpe
/n/rama/s5/dickson/euterpe/tools/bin/pd1cat
>-p
/n/rama/s5/dickson/euterpe/clockbias:/n/rama/s5/dickson/euterpe/gards/subb
loc
>ks:/n/rama/s5/dickson/euterpe/gards/dcell:/n/rama/s5/dickson/euterpe/pr
>ot
eus/gar
>ds/leaf:/n/rama/s5/dickson/euterpe/proteus/gards/sofa:/n/rama/s5/dickso
>n/
euterpe
>/proteus/gards/dcell `grep -v '^#' < guards/es-pass1.strength | awk
'{print $4;}'
> | \
>    sort | uniq | awk '{printf ("%s.pd1 ", $1)}'` >
guards/es-pass1.macros.te
>mp
>/n/rama/s5/dickson/euterpe/tools/bin/pd1cat: xbmux2dh32s.pd1 not found
>in
/n/ram
>a/s5/dickson/euterpe/clockbias:/n/rama/s5/dickson/euterpe/gards/subbloc
>ks
:/n/ram
>a/s5/dickson/euterpe/gards/dcell:/n/rama/s5/dickson/euterpe/proteus/gar
>ds
/leaf:/
>n/rama/s5/dickson/euterpe/proteus/gards/sofa:/n/rama/s5/dickson/euterpe
>/p
roteus/
>gards/dcell
>gmake[2]: *** [guards/es-pass1macros.pd1] Error 2
>gmake[2]: Leaving directory
~/N/rama/root/s5/dickson/euterpe/verilog/bsrc/es'
>gmake[1]: *** [es-base.netcap] Error 1
>gmake[1]: Leaving directory
~/N/rama/root/s5/dickson/euterpe/verilog/bsrc/es'
>gmake: *** [esguards] Error 1
>
>
>did something just change to cause this ?
>
>                                dickson
```

Rich, I don't know if anything changed or not, but the xbmux2dh24s and xbmux2dh32s are missing from the listed search path for pd1cat. Also, I could not find them in the /u/chip/... tree.

These might be new cells and the pdls may not have been generated yet.
Geert would know.

Thanks,
Dave

--
Dave Van't Hof vanthof@microunity.com MicroUnity Systems Engineering,
Inc.
"What rolls down stairs, alone or in pairs, rolls over the neighbor's dog?"

What's great for a snack and fits on your back? It's log, log, log!"
LOG from BLAMMO! (tm) All kids love Log! #include
<std_disclaim.h>

.

From: tbr
Sent: Thursday, September 29, 1994 11:00 AM
To: 'Mark Hofmann'
Cc: 'Alan Corry'
Subject: no PIFPACKing
Follow Up Flag: Follow up
Flag Status: Red

Mark Hofmann wrote (on Wed Sep 28):

Hi Tim,

Alan has a situation where for 3 sections of Euterpe he does not want to pifpack cells. He can get this effect by removing the "usepifpack" file, but ideally we would want to control this through use of a define in the Makefile. Did we have this set up at one time? One way to not pifpack something would be to say:

Well, we should check that the other rule which gets invoked when there is no usepifpack file is still up to date. Rich was doing this for a while (but has now gone back to packing) byt defining bothe these variables in the local Makefile (ie no need to have to specify them on the command line.

Removing the usepifpack file means (at least with the current setup in Makefile.share) that we'd have to duplicate the top level.

```
gmake PIFPACK_SQUEEZE=-I PIFPACK_DISTANCE=-I FOOgards
```

but perhaps we could make this a little more obvious with

```
USEPIFPACK=0
```

or some such.

We could modify the rules to put in an if at the shell level to test the value of such a variable, but it's then a little tricky to make sure things stop properly when there is an error.

How about some sort of . directive in the pim file which tells pifpack to be a no-op? Maybe we can't do this because there is no way to represent it in the .pif file, or perhaps it could be slipped back in by all that complicated awk stuff you have. This way would put all the information into the source file, rather than being a cobination of source file and Makefile. It could be similar to the way we handle the espresso stuff, where we grep something out of the source file to build the arguments for the command.

Tim

.

From: tbr
Sent: Thursday, September 29, 1994 11:11 AM
To: 'vant'
Cc: 'Geert Rosseel'; 'Mark Hofmann'; 'Dave Van't Hof'
Subject: Re: more topt questions :
Follow Up Flag: Follow up
Flag Status: Red

vant wrote (on Wed Sep 28):

Geert Rosseel writes:

I believe all of the errors you reported are caused by reading in a corrupted strength file.

For instance, when I look at the geert_euterge-iter.topt.log, there are many ERRORS that topt is spitting out:

```
*****  
                                ERROR! Instance gt/UgtSnake/UmuxCtl/Uahold_2/u0 (basename:  
xbor7) is being set to basename xbor5 from strength file at line 17588.  
    This is a very very bad thing to do!  
*****
```

This would cause the errors for missing pincaps, sdl errors, extra input pins, etc. This is a very very bad thing to have happen. Please check how the strength file is being generated.

The above error is caused when the gate type for a specific instance was changed. Ie, the strength file says that the gate is an OR5, but the edif netlist now says it's an OR7. Topt can not deal with this cleanly.

Topt sets the return code to 3 (bad input) because it is a bad input file, however, the -0 flag overrides this and will set the return code to 0. Maybe this should be changed?

Anyway, the data being fed to topt would cause all kinds of bad things to happen...

Hope this helps.

Looks like the dreaded inconsistency between top level and sub-block we discussed Wed morning.

Tim

From: Tim B. Robinson [tbr@aphrodite]
Sent: Thursday, September 29, 1994 11:11 AM
To: 'vant'
Cc: 'Geert Rosseel'; 'Mark Hofmann'; 'Dave Van't Hof'
Subject: Re: more topt questions :

vant wrote (on Wed Sep 28):

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Maybe this should be changed?

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happen...

Hope this helps.

Looks like the dreaded inconsistency between top level and sub-block we discussed Wed
morning.

Tim

.

From: tbr
Sent: Thursday, September 29, 1994 11:14 AM
To: 'Wayne Freitas'
Subject: Cerberus questions
Follow Up Flag: Follow up
Flag Status: Red

Wayne Freitas wrote (on Wed Sep 28):

Tim, I attending our on again, off again bring-up meeting with a couple of the software people and came away with pretty much the same action items that I got over 4 months ago.

Are you still planning on having Euterpe support a master/slave mode for the Cerberus Bus Interface tool.

Not suer what you mean here. Euterpe is a master, but all its registers are accessible as slaves to any other external master.

Can we force Euterpe to fetch from the Cerberus Bus address upon reset by forcing a special register to be set.

Not directly. Current plan endorsed by sotware folks is to have an initial ROM for bringup which essentially just branches to an address in cerberus space. It can then be kept constan while we develop boot code from the workstation cerberus slave.

Tim

.

From: tbr
Sent: Thursday, September 29, 1994 11:16 AM
To: 'Wayne Freitas'
Cc: 'graham@echidna'; 'lisar'; 'hestia@echidna'; 'jt@echidna'
Subject: FlashPROM Sockets for initial boards
Follow Up Flag: Follow up
Flag Status: Red

Wayne Freitas wrote (on Wed Sep 28):

To support the bring-up effort we need to be able to program the EEPROM's off of the mainboard. If I provide a socket to use does anybody have a problem with loading the initial PCA's with sockets in place of the EEPROM's

It's not clear we will need to make changes to the EEPROM off the board, though we do need an initial program in there before it's loaded on the board. We intend to make that initial program totally trivial, essentially just a branch that forces code to be fetched from cerberus space. We will have verified this specific configuration as part of the verification process before tapeout, so we would have no reason to expect a problem with this approach.

Tim

From: Tim B. Robinson [tbr@aphrodite]
Sent: Thursday, September 29, 1994 11:16 AM
To: 'Wayne Freitas'
Cc: 'graham@echidna'; 'lisar@aphrodite'; 'hestia@echidna'; 'jt@echidna'
Subject: FlashPROM Sockets for initial boards

Wayne Freitas wrote (on Wed Sep 28):

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Tim

.

From: Mark Hofmann [hopper@tomato]
Sent: Thursday, September 29, 1994 11:20 AM
To: 'Tim B. Robinson'
Subject: Re: top on godzilla

Tim B. Robinson writes:
Can you explain the following?

```
tbr@godzilla ~/euterpe/verilog/bsrc/rg/gards 427 % which top
/usr/local/bin/top
tbr@godzilla ~/euterpe/verilog/bsrc/rg/gards 428 % printenv PATH
/usr/local/pkg/ncd/bin:/n/auspex/s15/tbr/bin:/u/peter/bin/sun4:/u/peter/src/mverify/scripts../usr/ucb:/u/chip/tools/bin:/n/ram
r/bin/sunview1:/ushare/bin:/usr/hosts/etc:/usr/etc:/a/zycad.5.1a/XPLUS5.1a/bin:/a/zycad.5.1a/XPLUS5.1a/graphics/XPLUS/I
usr/vlsi.new/v8r3/bin:/a/octtools:/a/octtools/bin:/n/rama/s6/quad/exec/sun4:/n/iapetus/a/hspice
```

Looks like it ought to be seeing the one in /u/chip/tools first, but
it's not.

Oughter work. Have you rehashed?

-hopper

.

From: Wayne Freitas [wayne@echidna]
Sent: Thursday, September 29, 1994 12:05 PM
To: 'tbr@aphrodite'
Subject: Re: Cerberus questions

> From tbr@aphrodite Thu Sep 29 09:13:42 1994
> Date: Thu, 29 Sep 1994 09:13:38 -0700
> From: tbr@aphrodite (Tim B. Robinson)
> To: wayne@echidna (Wayne Freitas)
> Subject: Cerberus questions
> Content-Length: 861
>
>
> Wayne Freitas wrote (on Wed Sep 28):
>
>
> Tim, I attending our on again, off again bring-up meeting with a
> couple of the software people and came away with pretty much the same
> action items that I got over 4 months ago.
>
> Are you still planning on having Euterpe support a master/slave mode
> for the Cerberus Bus Interface tool.
>
> Not sure what you mean here. Euterpe is a master, but all its
> registers are accessible as slaves to any other external master.

In what has been referred to as "Serial Mode" on the Cerberus Bus Interface tool I need to control to SC. Is there any change here?

>
> Can we force Euterpe to fetch from the Cerberus Bus address upon reset
> by forcing a special register to be set.
>
> Not directly. Current plan endorsed by software folks is to have an
> initial ROM for bringup which essentially just branches to an address
> in cerberus space. It can then be kept constant while we develop boot
> code from the workstation cerberus slave.
>

We had talked earlier about being able to set a register in Euterpe which would cause Euterpe to fetch from Cerberus upon completing a reset instead of going out to the EEPROM. This would be accomplished by causing Cerberus to issue reset then going into Euterpe in some specified time period and setting this register. This approach gives us several advantages, first we only dependent on Cerberus lines (SD,SC), vs the EEPROM (Address, data and control) in getting a PCA to work. Second we don't have to program the EEPROM before it's installed onto the PCA, this really becomes a nuisance when we begin doing higher volumes. It means we have to buy a gang programmer and pull the parts from stock, label them put them back in, or arrange/pay our vendor to do the above. Third, if the EEPROM got corrupted we either have to design a fixture to program on the board or remove the component and replace it. I haven't the slightest idea how much of a problem this is to design in, but it really removes a couple of headaches when it comes to getting Hestia going in the bring-up and mfg. environment.

> Tim
>
>

From: lisa
Sent: Thursday, September 29, 1994 2:13 PM
To: 'software-checkins-dist'
Subject: gnu-tools/sim/terp execloop.c

Update of /p/cvsroot/gnu-tools/sim/terp
In directory calliope:/N/hyperion/root/sl/lisa/gnu-tools/sim/terp

Modified Files:
 execloop.c

Log Message:

emdepi needed some parentheses to get the mask right

.

From: Geert Rosseel [geert@ambiorix]
Sent: Thursday, September 29, 1994 2:22 PM
To: 'agc@ambiorix'; 'dickson@ambiorix'; 'hopper@ambiorix'; 'lisar@ambiorix'; 'mws@ambiorix'; 'tbr@ambiorix'; 'vanthof@ambiorix'; 'vo@ambiorix'; 'wampler@ambiorix'; 'woody@ambiorix'
Subject: Top-level route status

Hi,

I build a new toplevel of euterpe :

Included : cdio ctio0 ctio1 drio ck cp cj iq hc0 hc1 nb mst mc g f rg + custom blocks

Problems :

-> gt needs to be rebuild and placement needs to be adjusted.

It has not been rebuild in /u/chip since the instance name remapping. I could not include gt

-> cj has two instances sticking out beyond the 3148 limit for the left edge. I placed them by hand and proceeded to route.

instances are ***I3I4/U7 and ***I3I4/U8 in the middle control section

-> Routing took 2:50 hours : 998 unrouted wires

The xbhrdh24s cells have bad targets. That explains a lot of these unrouted wires.

-> 24274 paths don't meet timing

-> In many double cycle paths, the last hr cell is not part of design yet and topt thinks it's a regular path. This causes a lot of hr cells to grow.

For cdio and nb, we'll have to force the output levels.

All the data is in ~geert/chip/euterpe/verilog/bsrc/gards.save.

I am making a plot.

Plan for next top-level run :

```
* fix cj           : geert
* fix gt           : alan
* strip between d-cache & d-tag   : alan
* new cp           : rich
* strip between i-cache and i-tag : geert
* build es in /u/chip       : rich
* release new hc          : alan
* check sr origin and rebuild sr : ???
* add dr                : geert
```

The next top-level run is planned for Friday evening.

Gleert

.

From: tbe@MicroUnity.com
Sent: Thursday, September 29, 1994 2:37 PM
To: 'Kevin Peterson'
Cc: 'tbr'; 'wayne'; 'graham'; 'lisar'; 'hestia'; 'jt'; 'pmayer'
Subject: Re: FlashPROM Sockets for initial boards

>> It's not clear we will need to make changes to the EEPROM off the
>> board, though we do need an initial program in there before it's loaded
>> on the board. We intend to make that initial program totally trivial,
>> essentially just a branch that forces code to be fetched from cerberus
>> space. We will have verified this specific configuration as part of
>> the verification process before tapeout, so we would have no reason to
>> expect a problem with this approach.

>
> Ideally, there should be no programming changes to the EEPROM but
> inevitably, there will be. Why can't we use a PLCC package
> (e.g. AT29L010-20JC)? It can be socketed or surface mounted on the
> same pad footprint (but does require some extra clearance for the
> socket).

>
>-Kevin

The current package for the EEPROM is a T-WOP (.0198" pitch). I know of no
socket for such a package. There is precious little room under Euterpe on
the side where the I/O pads are for a larger package, as I suspect a PLCC
would be. Pattie is concerned about fitting the vias and traces as is, and
I am concerned about accommodating not just the PLCC but the socket. These
sockets that use the same land pattern are a mixed bag, in my experience.
They are somewhat fragile and although they use the original parts land
pattern, they can be hard to reflow and rework. Not a standalone reason
against using them for first units, but I doubt that they will fit. If
someone can identify an equivalent EEPROM in a PLCC, we can conclusively assess
fit.

-Tom

Tom Eich
MicroUnity Systems Engineering, Inc.
255 Caspian Dr. Sunnyvale, CA 94089
(408)734-8100, (408)734-8136 fax

tbe@microunity.com

From: sysadm@gaea on behalf of Bob Morgan [bobm@microunity.com]
Sent: Thursday, September 29, 1994 5:25 PM
To: 'euterpe@gaea'

I just checked in version 1.2 of the MicroArchitecture document. Thanks to all those who gave me comments on version 1.1. I haven't finished incorporating all the comments yet, but we are going to be releasing a new version of the book every week or so, and there have been some significant updates. The major changes are listed in the file changefile.mif.

The Makefile in /euterpe/doc will print out the book (type "gmake book"). If you would like me to give you a hardcopy, or a bound hardcopy, let me know.
Thanks,
Bob

From: Buffalo Chip [chip@rhea]
Sent: Thursday, September 29, 1994 5:32 PM
To: 'geert@rhea'
Subject: pager log message

page from chip to geert:

Release euterpe/verilog/bsrc/lt BOM 59.0 initiated by agc completed @ Thu Sep 29 15:31:13
PDT 1994 with exit status 0.. chip

From: Geert Rosseel [geert@rhea]
Sent: Thursday, September 29, 1994 5:52 PM
To: 'geert@rhea'
Subject: pager log, sender copy

```
page from geert to geert:
pageme gmake geert_euterpegards start:Sep_29_15:49 end: Sep_29_15:49 exit
1
```

[illegible]

From: Geert Rosseel [geert@rhea]
Sent: Thursday, September 29, 1994 5:52 PM
To: 'geert@rhea'
Subject: pager log, sender copy

page from geert to geert:
pageme gmake geert_euterpegards start:Sep_29_15:49 end: Sep_29_15:49 exit
1

lock open: Permission denied
all ports busy
lock open: Permission denied
all ports busy
lock open: Permission denied
all ports busy
lock open: Permission denied
all ports busy
lock open: Permission denied
all ports busy
all ports busy
all ports busy
all ports busy
all ports busy
all ports busy
all ports busy
all ports busy
all ports busy
all ports busy
all ports busy
all ports busy

From: Tim B. Robinson [tbr@aphrodite]
Sent: Thursday, September 29, 1994 6:06 PM
To: 'craig@aphrodite'
Cc: 'euterpe@aphrodite'
Subject: GTLB access

We have run into a problem with the GTLB mask field. When the LTLB was changed to implement only the XOR field, craig wanted the sense of the mask field inverting so that the LTLB mask would be read only with a value of 0 rather than all 1's. To be consistent with this, the GTLB definition was to be changed too, with the thinking being that all we had to do was reverse the sense of the data going in and out via the CMOS read/write ports. However, the GTLB physical array uses the same I/O pins for the mask and match arrays, effectively selecting between them with an additional address bit. So we cannot invert one without inverting the other unless we add more logic which we can ill afford in order to invert the data selectively.

I therefore propose that we go back to the original (and less confusing) definition, with the LTLB match field reading back always all 1's and no extra inversions in the GTLB path. I think this can still be justified as consistent with the general definition of reserved fields always reading zero, because this is not really a reserved field. It is the LTLB match field, which in this implementation happens to have a reserved *value* of all 1's which you can't change.

Comments please - and remember atoms are at stake!

Tim

From: Charlie Root [root@godzilla]
Sent: Thursday, September 29, 1994 6:09 PM
To: 'geert@godzilla'
Subject: Output from "at" job

Your "at" job "6054" produced the following output:

```
Working cell: euterpe
PDF file for plotting: /u/geert/chip/proteus/tools/lib/hyperplot/p691.pdf

Current working directory: /n/tmp/plot
Current Layout: euterpe
/u/geert/chip/proteus/tools/bin/cifles -r -l M2 -l M3 -l M4 -l TEXT -s
0.05 -n /dev/null -v
/n/auspex/s14/geert/chip/euterpe/verilog/bsrc/gards/tmp.boo -c euterpe -o
euterpe.22277
Processing cell
/n/auspex/s14/geert/chip/euterpe/verilog/bsrc/gards/euterpe.ly
Processing cell
/n/auspex/s14/geert/chip/euterpe/verilog/bsrc/gards/chunk554_euterpe.ly
Processing cell
/n/auspex/s14/geert/chip/euterpe/proteus/compass/layouts/via23.ly
Processing cell
/n/auspex/s14/geert/chip/euterpe/proteus/compass/layouts/via34.ly
Processing cell
/n/auspex/s14/geert/chip/euterpe/proteus/compass/layouts/via12.ly
Processing cell
/n/auspex/s14/geert/chip/euterpe/proteus/compass/leaf/xbmux2dh2s.ly
Processing cell
/n/auspex/s14/geert/chip/euterpe/proteus/compass/layouts/mobieclium.ly
Processing cell
/n/auspex/s14/geert/chip/euterpe/proteus/compass/layouts/isrc.ly
Processing cell
/n/auspex/s14/geert/chip/euterpe/proteus/compass/layouts/bjt1.ly
Processing cell
/n/auspex/s14/geert/chip/euterpe/proteus/compass/layouts/pld.ly
Processing cell
/n/auspex/s14/geert/chip/euterpe/proteus/compass/layouts/unupld_lobe.ly
Processing cell
/n/auspex/s14/geert/chip/euterpe/proteus/compass/layouts/mobieclium_lobe.l
y
Processing cell
/n/auspex/s14/geert/chip/euterpe/proteus/compass/layouts/unuiscr_lobe.ly
Processing cell
/n/auspex/s14/geert/chip/euterpe/proteus/compass/layouts/isrc_lobe.ly
Processing cell
/n/auspex/s14/geert/chip/euterpe/proteus/compass/layouts/ef2x1.ly
Processing cell
/n/auspex/s14/geert/chip/euterpe/proteus/compass/layouts/mux2x1.ly
Processing cell
/n/auspex/s14/geert/chip/euterpe/proteus/compass/layouts/isrc2.ly
Processing cell
/n/auspex/s14/geert/chip/euterpe/proteus/compass/layouts/pld_lobe.ly
Processing cell
/n/auspex/s14/geert/chip/euterpe/proteus/compass/layouts/contact.ly
Processing cell
/n/auspex/s14/geert/chip/euterpe/proteus/compass/leaf/xbhrdf2s.ly
Processing cell
/n/auspex/s14/geert/chip/euterpe/proteus/compass/leaf/xbor4df2s.ly
Processing cell
/n/auspex/s14/geert/chip/euterpe/proteus/compass/layouts/or4.ly
Processing cell
/n/auspex/s14/geert/chip/euterpe/proteus/compass/layouts/buf1x1.ly
```


Processing cell
/n/auspex/s14/geert/chip/euterpe/proteus/compass/leaf/xbmux2df16s.1y
Processing cell
/n/auspex/s14/geert/chip/euterpe/proteus/compass/layouts/unubjt1.1y
Processing cell
/n/auspex/s14/geert/chip/euterpe/proteus/compass/layouts/buflx2.1y
Processing cell
/n/auspex/s14/geert/chip/euterpe/proteus/compass/leaf/xbffdh6s.1y
Processing cell
/n/auspex/s14/geert/chip/euterpe/proteus/compass/layouts/lat1x1.1y
Processing cell
/n/auspex/s14/geert/chip/euterpe/proteus/compass/leaf/xbor6df6s.1y
Processing cell
/n/auspex/s14/geert/chip/euterpe/proteus/compass/layouts/or6.1y
Processing cell
/n/auspex/s14/geert/chip/euterpe/proteus/compass/leaf/xbor5df4s.1y
Processing cell
/n/auspex/s14/geert/chip/euterpe/proteus/compass/layouts/or5.1y
Processing cell
/n/auspex/s14/geert/chip/euterpe/proteus/compass/leaf/xbhrdh2s.1y
Processing cell
/n/auspex/s14/geert/chip/euterpe/proteus/compass/leaf/xbor6df4s.1y
Processing cell
/n/auspex/s14/geert/chip/euterpe/proteus/compass/leaf/xbor5df2s.1y
Processing cell
/n/auspex/s14/geert/chip/euterpe/proteus/compass/leaf/xbor9dh2s.1y
Processing cell
/n/auspex/s14/geert/chip/euterpe/proteus/compass/layouts/or9.1y
Processing cell
/n/auspex/s14/geert/chip/euterpe/proteus/compass/leaf/xbffdh12s.1y
Processing cell
/n/auspex/s14/geert/chip/euterpe/proteus/compass/layouts/lat1x2.1y
Processing cell
/n/auspex/s14/geert/chip/euterpe/proteus/compass/leaf/xbhrdf24s.1y
Processing cell
/n/auspex/s14/geert/chip/euterpe/proteus/compass/leaf/xbmux2df12s.1y
Processing cell
/n/auspex/s14/geert/chip/euterpe/proteus/compass/leaf/xbhrdh24s.1y
Processing cell
/n/auspex/s14/geert/chip/euterpe/proteus/compass/leaf/xbor4df4s.1y
Processing cell
/n/auspex/s14/geert/chip/euterpe/proteus/compass/leaf/xbffedh2s.1y
Processing cell
/n/auspex/s14/geert/chip/euterpe/proteus/compass/leaf/xbhrdh3s.1y
Processing cell
/n/auspex/s14/geert/chip/euterpe/proteus/compass/leaf/xbc01df2s.1y
Processing cell
/n/auspex/s14/geert/chip/euterpe/proteus/compass/leaf/xbc01df4s.1y
Processing cell
/n/auspex/s14/geert/chip/euterpe/verilog/bsrc/gards/chunk555_euterpe.1y
Processing cell
/n/auspex/s14/geert/chip/euterpe/proteus/compass/leaf/xbffedh6s.1y
Processing cell
/n/auspex/s14/geert/chip/euterpe/proteus/compass/leaf/xbhrdf4s.1y
Processing cell
/n/auspex/s14/geert/chip/euterpe/proteus/compass/leaf/xbhrdf12s.1y
Processing cell
/n/auspex/s14/geert/chip/euterpe/verilog/bsrc/gards/chunk556_euterpe.1y
Processing cell
/n/auspex/s14/geert/chip/euterpe/verilog/bsrc/gards/chunk557_euterpe.1y
Processing cell
/n/auspex/s14/geert/chip/euterpe/verilog/bsrc/gards/chunk558_euterpe.1y
Processing cell
/n/auspex/s14/geert/chip/euterpe/verilog/bsrc/gards/chunk559_euterpe.1y
Processing cell
/n/auspex/s14/geert/chip/euterpe/verilog/bsrc/gards/chunk560_euterpe.1y
Processing cell
/n/auspex/s14/geert/chip/euterpe/verilog/bsrc/gards/chunk561_euterpe.1y

Processing cell
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Processing cell

[illegible]

```

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Processing cell
/n/auspex/s14/geert/chip/euterpe/verilog/bsrc/gards/chunk1846_euterpe.ly
Creating euterpe.22277
Creating node name file /dev/null
ERROR! illegal subscript usage in rwl_an0p1600v[91
ERROR! illegal subscript usage in rwl_an0p1600v[91
ERROR! illegal subscript usage in rwl_an0p1600v[91
ERROR! illegal subscript usage in rwl_an0p1600v[91
ERROR! illegal subscript usage in rwl_an0p1600v[91
ERROR! illegal subscript usage in rwl_an0p1600v[91
Freed Nodes: 0    Peek Nodes: 43654
Freed Boxes: 0    Peek Boxes: 531231
Freed Polys: 0    Peek Polys: 2305
Freed Wires: 0    Peek Wires: 0

CLI contents:
-cif_tm -localdir /n/tmp/plot -p ce3436 -d
u/geert/chip/proteus/tools/lib/hyperplot/p691.pdf -t ciftopcell -af -h
2.0 -c 1 euterpe.22277

```

[1] 22439
hostid set to 0x55416d20

HyperPlot - V2.0h
29-Sep-1994 15:17:35
Copyright (c) 1993 - Pinebush Technologies, Inc.
Proprietary and Confidential to Pinebush Technologies, Inc.

Configuration Options:

Auto_strip : on
Overlap : 0.00
Max strips : 99
Max layers : 1023
Text width : 4
Display_array : N/A
Top cell method : input_file_name
Plot empty plots : no
Username label : off
Legend: R/H , Axis: -BL- , Label: RC
Regions: Top off , Bottom off , Left off , Right 4.00

Processing file 'euterpe.22277'

Output options:

plotter : ce3436
routing : direct
queue : /dev/vp0
raster format : joined
plotter host : plotter

Parameters:

Chip - euterpe.22277
PDF file - /u/geert/chip/proteus/tools/lib/hyperplot/p691.pdf
Top symbol - ciftopcell
Plot to level - All levels
Window - None
Text - 2.00
Copies - 1

Layers to be processed: ALGN,BUR,NWEL,PWEL,BUCT,EMIT,COLL,BPL1,BACT,NACT
PACT,ENH,DEP,PPL1,NPL1,P1SL,DRES,UPL1,SDEC,CTPG
M1,V12,M2,V23,M23P,M3,V34,M34P,M4,V45,M5,MS1
VS12,MS2,VS23,MS3,GRID,OPTD,SOFA,OBS1,OBS2,OBS3
POBS,TEXT,BBOX,F010,F020,F030,F040,F050,F060
F070,F080,F090,F100,F110,F120,F130,F140,F150
F160,F170,F180,F190,F200,F210,F220,F230,F240
F250,F260,F270,F280

Current scaling parameters:

Plot height will be scaled to plotter maximum.
Plot will be rotated if necessary.
Plot will not be mirrored.

Reading layout data from euterpe.22277

Cif Warning: Unsupported user extension (4I) ignored

Cif Warning: Unsupported user extension (4R) ignored

hostid set to 0x7140171e

Read finished, tree size: 22832128 bytes, cpu: 00:02:49

Analyzing tree from ciftopcell

Tree analysis finished, cpu: 00:00:25

Creating rasterfile: /n/tmp/plot/hyperplot.raster.22441

black: rasterized 36073352 vectors, 0 trapezoids, 0 rectangles

cyan: rasterized 30238233 vectors, 0 trapezoids, 6981042 rectangles
magenta: rasterized 9266532 vectors, 0 trapezoids, 2824587 rectangles
yellow: rasterized 39504765 vectors, 0 trapezoids, 20096236 rectangles

Plot completed -- cpu: 00:38:08

Directly sending rasterfile:/n/tmp/plot/hyperplot.raster.22441 to plotter.
Check logfile: hypersend.log

HyperPlot completed -- cpu: 00:41:22
[1] + Done (/usr/local/bin/hostid 0x55416d20; sleep 15;
hostid \$retid)
chmod: cli.lst: Not owner
chmod: history.logs: Not owner
chmod: hyperplot.raster.16177: Not owner

.

From: tbr
Sent: Thursday, September 29, 1994 6:14 PM
To: 'Mark Hofmann'
Subject: Re: top on godzilla
Follow Up Flag: Follow up
Flag Status: Red

Mark Hofmann wrote (on Thu Sep 29):

/u/chip/tools/bin/top should do the Right Thing now.

Can you explain the following?

```
tbr@godzilla ~/euterpe/verilog/bsrc/rg/gards 427 % which top
/usr/local/bin/top
tbr@godzilla ~/euterpe/verilog/bsrc/rg/gards 428 % printenv PATH
/usr/local/pkg/ncd/bin:/n/auspex/s15/tbr/bin:/u/peter/bin/sun4:/u/peter/src/mverify/scripts../usr/ucb:/u/chip/tools/bin:/n/rama/s
```

Looks like it ought to be seeing the one in /u/chip/tools first, but
it's not.

Tim

From: sysadm@gaea on behalf of Guillermo A. Loyola [gmo@microunity.com]
Sent: Thursday, September 29, 1994 6:16 PM
To: 'euterpe@gaea'

In article <199409292305.QAA15547@aphrodite.microunity.com>, tbr@aphrodite.microunity.com (Tim B. Robinson) writes:

>
> I therefore propose that we go back to the original (and less
> confusing) definition, with the LTLB match field reading back always
> all 1's and no extra inversions in the GTLB path.

Sounds great, we (software) love your propossal.

|> ... It is the LTLB match field, which in this
 ^^^^^^

You mean mask field, right?

Gmo.

.

From: tbr
Sent: Thursday, September 29, 1994 6:19 PM
To: 'Wayne Freitas'
Subject: Re: Cerberus questions
Follow Up Flag: Follow up
Flag Status: Red

Wayne Freitas wrote (on Thu Sep 29):

> From tbr@aphrodite Thu Sep 29 09:13:42 1994
> Date: Thu, 29 Sep 1994 09:13:38 -0700
> From: tbr@aphrodite (Tim B. Robinson)
> To: wayne@echidna (Wayne Freitas)
> Subject: Cerberus questions
> Content-Length: 861
>
>
> Wayne Freitas wrote (on Wed Sep 28):
>
>
> Tim, I attending our on again, off again bring-up meeting with a
> couple of the software people and came away with pretty much the same
> action items that I got over 4 months ago.
>
> Are you still planning on having Euterpe support a master/slave mode
> for the Cerberus Bus Interface tool.
>
> Not suer what you mean here. Euterpe is a master, but all its
> registers are accessible as slaves to any other external master.

In what has been refered to as "Serial Mode" on the Cerberus Bus Interface tool I need to control to SC. Is there any change here?

No change in euterpe. I think the issue was that craig would prefer for the clock to always run at nominal rate and for the interface device to insert wait states if it can't keep up. However, this is just an issue of whether we are willing to cut thin internal clock loop for bringup.

>
> Can we force Euterpe to fetch from the Cerberus Bus address upon reset
>
> by forcing a special register to be set.
>
> Not directly. Current plan endorsed by sotware folks is to have an
> initial ROM for bringup which essentially just branches to an address
> in cerberus space. It can then be kept constan while we develop boot
> code from the workstation cerberus slave.
>

We had talked earlier about being able to set a register in Euterpe which would cause Euterpe to fetch from Cerberus upon completing a reset instead of going out to the EEPROM. This would be accomplished by causing Cerberus to issue reset then going into Euterpe in some specified time period and setting this register. This approach gives

us several advantages, first we only dependent on Cerberus lines (SD,SC), vs the EEPROM (Address, data and control) in getting a PCA to work. Second we don't have to program the EEPROM before it's installed onto the PCA, this really becomes a nuisance when we begin doing higher volumes. It means we have to buy a gang programmer and pull the parts from stock, label them put them back in, or arrange/pay our vendor to do the above. Third, if the EEPROM get corrupted we either have to design a fixture to program on the board or remove the component and replace it. I haven't the slightest idea how much of a problem this is to design in, but it really removes a couple of headaches when it come to getting Hestia going in the bring-up and mfg. environment.

Long term though, would you be happy to have to have a Cerberus emulator for every box we want to bring up rather than using a gang programmer?

Tim

From: craig
Sent: Thursday, September 29, 1994 7:00 PM
To: 'wayne@echidna'
Subject: Re: Cerberus question

Euterpe has a watchdog timer, which can be set for a very long delay. Cerberus specifies a timeout delay, which is used for discovering whether a Cerberus device exists at a given address; this limits the number of idle cycles between a request and response. A Cerberus transaction can be delayed an arbitrary amount by hanging up the transmission of the final byte of the request, without causing a Cerberus timeout; in this case the bus is not idle (except for a small number of cycles) between request and response.

Craig

From: Buffalo Chip [chip@gamorra]
Sent: Thursday, September 29, 1994 7:13 PM
To: 'geert@gamorra'
Subject: output of euterpe/verilog/bsrc/cj/.checkoutrc

The output from euterpe/verilog/bsrc/cj/.checkoutrc is 144k, so it is not included in this mail message. Instead, check the file

/n/tmp/chiplog/geert.gamorra.1138.euterpe-verilog-bsrc-cj

(which is accessible from all machines). This file will disappear in about 5 days.

By the way, the exit status returned by .checkoutrc was 0.

From: Buffalo Chip [chip@rhea]
Sent: Thursday, September 29, 1994 7:14 PM
To: 'geert@rhea'
Subject: pager log message

page from chip to geert:

Release euterpe/verilog/bsrc/cj BOM 57.0 initiated by geert completed @ Thu Sep 29
17:13:02 PDT 1994 with exit status 0.. chip

From: tbr
Sent: Thursday, September 29, 1994 10:22 PM
To: 'Geert Rosseel'
Cc: 'agc@ambiorix'; 'dickson@ambiorix'; 'hopper@ambiorix'; 'lisar@ambiorix'; 'mws@ambiorix'; 'vanthof@ambiorix'; 'vo@ambiorix'; 'wampler@ambiorix'; 'woody@ambiorix'
Subject: Top-level route status
Follow Up Flag: Follow up
Flag Status: Red

Geert Rosseel wrote (on Thu Sep 29):

Hi,

I build a new toplevel of euterpe :

Included : cdio ctio0 ctio1 drio ck cp cj iq hc0 hc1 nb mst mc gf rg + custom blocks

Problems :

-> gt needs to be rebuild and placement needs to be adjusted.
It has not been rebuild in /u/chip since the instance name remapping. I could not include gt

-> cj has two instances sticking out beyond the 3148 limit
for the left edge. I placed them by hand and proceeded to route.

instances are ***I3I4/U7 and ***I3I4/U8 in the middle control section

-> Routing took 2:50 hours : 998 unrouted wires
The xbhrdh24s cells have bad targets. That explains a lot of these unrouted wires.

-> 24274 paths don't meet timing

This is bad. It's double the number we get in pass1 on the full top level. Given we should only expect timing trouble on interface nets something has to be wrong. Are you sure the top level was timed with the same cycle time we are using for the sub-blocks.

-> In many double cycle paths, the last hr cell is not part of design yet and topt thinks it's a regular path. This causes a lot of hr cells to grow.
For cdio and nb, we'll have to force the output levels.

All the data is in ~geert/chip/euterpe/verilog/bsrc/gards.save.
I am making a plot.

Plan for next top-level run :

* fix cj : geert
* fix gr : alan
* strip between d-cache & d-tag : alan
* new cp : rich
* strip between i-cache and i-tag : geert
* build es in /u/chip : rich
* release new hc : alan
* check sr origin and rebuild sr : ???
* add dr : geert

The next top-level run is planned for Friday evening.

Tim

From: Tim B. Robinson [tbr@aphrodite]
Sent: Thursday, September 29, 1994 10:22 PM
To: 'Geert Rosseel'
Cc: 'agc@ambiorix'; 'dickson@ambiorix'; 'hopper@ambiorix'; 'lisar@ambiorix'; 'mws@ambiorix'; 'vanthof@ambiorix'; 'vo@ambiorix'; 'wampler@ambiorix'; 'woody@ambiorix'
Subject: Top-level route status

Geert Rosseel wrote (on Thu Sep 29):

Hi,

I build a new toplevel of euterpe :

Included : cdio ctio0 ctio1 drio ck cp cj iq hc0 hcl nb mst mc gf rg
+ custom blocks

Problems :

- > gt needs to be rebuild and placement needs to be adjusted.
It has not been rebuild in /u/chip since the instance name remapping. I could not include gt
- > cj has two instances sticking out beyond the 3148 limit
for the left edge. I placed them by hand and proceeded to route.

instances are ***I3I4/U7 and ***I3I4/U8 in the middle control section
- > Routing took 2:50 hours : 998 unrouted wires
The xbhrrdh24s cells have bad targets. That explains a lot of these unrouted wires.
- > 24274 paths don't meet timing

This is bad. It's double the number we get in pass1 on the full top level. Given we should only expect timing trouble on interface nets something has to be wrong. Are you sure the top level was timed with the same cycle time we are using for the sub-blocks.

- > In many double cycle paths, the last hr cell is not part of design
yet and topt thinks it's a regular path. This causes a lot of
hr cells to grow.
For cdio and nb, we'll have to force the output levels.

All the data is in -geert/chip/euterpe/verilog/bsrc/gards.save.
I am making a plot.

Plan for next top-level run :

* fix cj	: geert
* fix gt	: alan
* strip between d-cache & d-tag	: alan
* new cp	: rich
* strip between i-cache and i-tag	: geert
* build es in /u/chip	: rich
* release new hc	: alan
* check sr origin and rebuild sr	: ???
* add dr	: geert

The next top-level run is planned for Friday evening.

.

From: tbr
Sent: Thursday, September 29, 1994 10:32 PM
To: 'dickson'; 'mws'
Cc: 'craig'
Subject: forwarded message from Craig Hansen
Follow Up Flag: Follow up
Flag Status: Red

OK, so what do we need to do to be able to accomplish this?

I assume the intent here is that the start vector is always the same, but that depending on the Cerberus address, some shuffling of Cerberus vs flash address spaces needs to take place. Alternatively, we make the atsr vector a function of the cerberus address.

Craig, exactly what do you have in mind? Current mapping is as documented in the micro-arch some time back.

Tim

----- Start of forwarded message -----

Return-Path: <craig@mnemosyne>

Received: from aphrodite.microunity.com by gaea.microunity.com (4.1/muse1.3)
id AA15761; Thu, 29 Sep 94 13:31:23 PDT

Received: from mnemosyne.microunity.com by aphrodite.microunity.com (8.6.4/muse-sw.2)
id NAA15003; Thu, 29 Sep 1994 13:31:19 -0700

Received: from localhost by mnemosyne.microunity.com (8.6.4/muse-sw.2)
id NAA17860; Thu, 29 Sep 1994 13:31:16 -0700

Message-Id: <199409292031.NAA17860@mnemosyne.microunity.com>

From: craig@mnemosyne (Craig Hansen)

To: tbr@aphrodite, wayne@echidna

Cc: graham@echidna, hestia@echidna, jt@echidna, lisar@aphrodite

Subject: Re: FlashPROM Sockets for initial boards

Date: Thu, 29 Sep 1994 13:31:16 -0700

A socket for the EEPROM should not be required. Euterpe must be able to boot from Cerberus directly by configuring the Cerberus address of Euterpe.

Craig

----- End of forwarded message -----

.

From: tbr
Sent: Thursday, September 29, 1994 10:44 PM
To: 'Bob Morgan'
Follow Up Flag: Follow up
Flag Status: Red

Bob Morgan wrote (on Thu Sep 29):

I just checked in version 1.2 of the MicroArchitecture document. Thanks to all those who gave me comments on version 1.1. I haven't finished incorporating all the comments yet, but we are going to be releasing a new version of the book every week or so, and there have been some significant updates. The major changes are listed in the file changefile.mif.

The Makefile in /euterpe/doc will print out the book (type "gmake book"). If you would like me to give you a hardcopy, or a bound hardcopy, let me know.

Good stuff. Please run me a bound hard copy each time there is a major release.

Thanks
Tim

From: Tim B. Robinson [tbr@aphrodite]
Sent: Thursday, September 29, 1994 10:46 PM
To: 'gmo@microunity.com'
Cc: 'euterpe@gaea'

Guillermo A. Loyola wrote (on Thu Sep 29):

In article <199409292305.QAA15547@aphrodite.microunity.com>, tbr@aphrodite.microunity.com (Tim B. Robinson) writes:

```
>  
> I therefore propose that we go back to the original (and less  
> confusing) definition, with the LTLB match field reading back always  
> all 1's and no extra inversions in the GTLB path.
```

Sounds great, we (software) love your propossal.

```
|> ... It is the LTLB match field, which in this  
      ^^^^^
```

You mean mask field, right?

Oops. Yes.

Tim

.

From: tbr
Sent: Thursday, September 29, 1994 10:49 PM
To: 'Mark Hofmann'
Subject: Re: top on godzilla
Follow Up Flag: Follow up
Flag Status: Red

Mark Hofmann wrote (on Thu Sep 29):

Tim B. Robinson writes:
Can you explain the following?

```
tbr@godzilla ~/euterpe/verilog/bsrc/rg/gards 427 % which top
/usr/local/bin/top
tbr@godzilla ~/euterpe/verilog/bsrc/rg/gards 428 % printenv PATH
/usr/local/pkg/ncd/bin:/n/auspex/s15/tbr/bin:/u/peter/bin/sun4:/u/peter/src/mverify/scripts:/usr/ucb:/u/chip/tools/bin:/n/rar
r/bin/sunview1:/ushare/bin:/usr/hosts:/etc:/usr/etc:/a/zycad.5.1a/XPLUS5.1a/bin:/a/zycad.5.1a/XPLUS5.1a/graphics/XPLUS/I
usr/vlsi.new/v8r3/bin:/a/octtools:/a/octtools/bin:/n/rama/s6/quad/exec/sun4:/n/iapetus/a/hspice
```

Looks like it ought to be seeing the one in /u/chip/tools first, but
it's not.

Oughter work. Have you rehashed?

No, how stupid. I was about to do it then I figured that since I had
not changed the path I didn't need to!.

Works now.

Tim

From: vant [vanthof@hestia]
Sent: Friday, September 30, 1994 9:33 AM
To: 'Tom Vo'; 'Geert Rosseel'
Cc: 'Dave Van't Hof'; 'Mark Hofmann'; 'Tim B. Robinson'; 'Lisa Robinson'
Subject: euterpe lvs finished.

The euterpe lvs finished and it's not exactly clean. The good news is there is no power/ground short. The bad news is:

NUMBER OF UN-MATCHED SCHEMATICS DEVICES	=	12023
NUMBER OF UN-MATCHED LAYOUT DEVICES	=	327
NUMBER OF MATCHED SCHEMATICS DEVICES	=	937387
NUMBER OF MATCHED LAYOUT DEVICES	=	937387

There are lots of extra schematic devices, so some block(s) is(are) missing from the layout that are in the schematic. I did notice that there seems to be large numbers of missing VII36 connections in the layout. Is there some block in knobdomain 36 missing?

The output is in
/u/vanthof/compass/mobi/euterpe/euterpe.compare/euterpe.lvs

Let me know if there is anything I can help with.

I've started up a fullchip ISS lvs on euterpe and it's running a lot slower than I thought. I'm working on this. In addition, I ran the IOBYTE through ISS and it's not clean. What's strange is that the calliope0 iobyte is clean.

More later.

Dave
--
Dave Van't Hof vanthof@microunity.com MicroUnity Systems Engineering,
Inc.
"What rolls down stairs, alone or in pairs, rolls over the neighbor's dog?"

What's great for a snack and fits on your back? It's log, log, log!"
LOG from BLAMMO! (tm) All kids love Log! #include
<std_disclaim.h>

From: Geert Rosseel [geert@rhea]
Sent: Friday, September 30, 1994 9:54 AM
To: 'geert@rhea'
Subject: pager log, sender copy

page from geert to geert:

pageme gmake geert_euterpegards start:Sep_30_06:56 end: Sep_30_07:51 exit

1

.

From: tbr
Sent: Friday, September 30, 1994 10:37 AM
To: 'vant'
Cc: 'Geert Rosseel'; 'Mark Hofmann'; 'Lisa Robinson'; 'Dave Van't Hof'; 'Tom Vo'
Subject: euterpe lvs finished.
Follow Up Flag: Follow up
Flag Status: Red

vant wrote (on Fri Sep 30):

The euterpe lvs finished and it's not exactly clean. The good news is there is no power/ground short. The bad news is:

```
NUMBER OF UN-MATCHED SCHEMATICS DEVICES  = 12023
NUMBER OF UN-MATCHED LAYOUT DEVICES    = 327
NUMBER OF MATCHED SCHEMATICS DEVICES    = 937387
NUMBER OF MATCHED LAYOUT DEVICES        = 937387
```

There are lots of extra schematic devices, so some block(s) is(are) missing from the layout that are in the schematic. I did notice that there seems to be large numbers of missing VII36 connections in the layout. Is there some block in knobdomain 36 missing?

As far as I can tell 36 is just a regular sofa knob (ie not to a custom block). Maybe something went wrong with the knobmap patching up.

The output is in /u/vanthof/compass/mobi/euterpe/euterpe.compare/euterpe.lvs

Let me know if there is anything I can help with.

I've started up a fullchip ISS lvs on euterpe and it's running a lot slower than I thought. I'm working on this. In addition, I ran the IOBYTE through ISS and it's not clean. What's strange is that the calliope0 iobyte is clean.

From: Tim B. Robinson [tbr@aphrodite]
Sent: Friday, September 30, 1994 10:37 AM
To: 'vant'
Cc: 'Geert Rosseel'; 'Mark Hofmann'; 'Lisa Robinson'; 'Dave Van't Hof'; 'Tom Vo'
Subject: euterpe lvs finished.

vant wrote (on Fri Sep 30):

The euterpe lvs finished and it's not exactly clean. The good news is there is no power/ground short. The bad news is:

NUMBER OF UN-MATCHED SCHEMATICS DEVICES	=	12023
NUMBER OF UN-MATCHED LAYOUT DEVICES	=	327
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NUMBER OF MATCHED LAYOUT DEVICES	=	937387

There are lots of extra schematic devices, so some block(s) is(are) missing from the layout that are in the schematic. I did notice that there seems to be large numbers of missing VII36 connections in the layout. Is there some block in knobdomain 36 missing?

As far as I can tell 36 is just a regular sofa knob (ie not to a custom block). Maybe something went wrong with the knobmap patching up.

The output is in
/u/vanthof/compass/mobi/euterpe/euterpe.compare/euterpe.lvs

Let me know if there is anything I can help with.

I've started up a fullchip ISS lvs on euterpe and it's running a lot slower than I thought. I'm working on this. In addition, I ran the IOBYTE through ISS and it's not clean. What's strange is that the calliope0 iobyte is clean.

From: Tim B. Robinson [tbr@aphrodite]
Sent: Friday, September 30, 1994 10:50 AM
To: 'euterpe@aphrodite'
Cc: 'tbr@aphrodite'; 'bobm@aphrodite'
Subject: debugger interrupt support

There has been a strong request to be able to cause an event in euterpe from an external Cerberus master to support bringup and debug. We will implement this using bit 61 of cerberus octlet 6 (defined as the unimplemented self test bit), which assignment has craig's blessing. Setting this bit will result in bit 1 of the event register being set. Acknowledging this event will require rewriting Cerberus octlet 6 to clear the bit there before clearing bit 1 in the event register.

When not required to support debug in this way (ie assuming bit 61 in octlet 6 is always 0), bit 1 of the event register can be used for normal interrupts from Calliope.

Tim

.

From: tbr
Sent: Friday, September 30, 1994 10:59 AM
To: 'dickson'; 'agc'; 'woody'
Subject: interrupts from cerberus
Follow Up Flag: Follow up
Flag Status: Red

Rich, can you figure out how to do this please? I think all we need is to take bit 61 from octlet 6 and or it into bit 1 of the forceval input to sr. You may need a synchronizer. I would also like this to get ored with the extra padding input alan defined ot allow us to get interrupts from an external PCMCIA adapter chip if we ever needed to. Again it seems like a simple OR function on the cmos side could do this. (Jay, we need to be sure the main board netlist has that pin strapped to the inactive state.)

There has been a strong request to be able to cause an event in euterpe from an external Cerberus master to support bringup and debug. We will implement this using bit 61 of cerberus octlet 6 (defined as the unimplemented self test bit), which assignment has craig's blessing. Setting this bit will result in bit 1 of the event register being set. Acknowledging this event will require rewriting Cerberus octlet 6 to clear the bit there before clearing bit 1 in the event register.

When not required to support debug in this way (ie assuming bit 61 in octlet 6 is always 0), bit 1 of the event register can be used for normal interrupts from Calliope.

From: sysadm@gaea on behalf of Jeff Marr [jeffm@microunity.com]
Sent: Friday, September 30, 1994 11:06 AM
To: 'euterpe@gaea'

In article <199409292305.QAA15547@aphrodite.microunity.com>,
tbr@aphrodite.microunity.com (Tim B. Robinson) writes:

```
>  
> We have run into a problem with the GTLB mask field. When the LTLB  
> was changed to implement only the XOR field, craig wanted the sense  
> of the mask field inverting so that the LTLB mask would be read only  
> with a value of 0 rather than all 1's. To be consistent with this,  
> the GTLB definition was to be changed too, with the thinking being  
> that all we had to do was reverse the sense of the data going in and  
> out via the CMOS read/write ports. However, the GTLB physical array  
> uses the same I/O pins for the mask and match arrays, effectively  
> selecting between them with an additional address bit. So we cannot  
> invert one without inverting the other unless we add more logic which  
> we can ill afford in order to invert the data selectively.  
>  
> I therefore propose that we go back to the original (and less  
> confusing) definition, with the LTLB match field reading back always  
> all 1's and no extra inversions in the GTLB path. I think this can  
> still be justified as consistent with the general definition of  
> reserved fields always reading zero, because this is not really a  
> reserved field. It is the LTLB match field, which in this  
> implementation happens to have a reserved *value* of all 1's which  
> you can't change.  
>  
> Comments please - and remember atoms are at stake!  
>  
> Tim  
>  
>  
This is good for verification. Less confusing makes test writing and debug simpler, plus,  
to a slight degree, this simplifies the mask generation code in the tests written in  
assembly.
```

--
Jeff "Won't you be my 'electronic neighbor?" Marr

From: Jay Tomlinson [woody@melpomene]
Sent: Friday, September 30, 1994 11:09 AM
To: 'Jeff Marr'
Cc: 'gmo@melpomene'; 'euterpe@melpomene'
Subject: illegal address exceptions

Jeff Marr wrote (on Fri Sep 30):

Jay Tomlinson writes:

> Jeff,
>
> You asked me earlier about illegal address exceptions. I looked at the code to
> be sure and as I suspected, this type exception will not prevent a register file
> write and it will not inhibit an NB request.
> The cases covered are:
> 680..0 - 7f..f (between cerberus and on-chip)
> pa[63:48] ~= 0
> pa[47] & not (one of the on-chip resources listed in the memory map)
>
> Let me know if you need more information.
>
> Jay
What is going to happen when the NB request completes? What are the side
affects?

Thankx,

jeffm

The NB request won't complete, because as far as I know these illegal address are not recognized by any of the NB peripherals. This means that there is now 1 less NB entry available.

The assumption here is that a reset must be done after this exception.

This is intended as a debug aid. That is what gmo said when he request that we change this from a machine check to an exception. This change was request made so that SW could find the problem by looking at the exception information.

Jay

.

From: tbr
Sent: Friday, September 30, 1994 11:15 AM
To: 'Jay Tomlinson'
Cc: 'euterpe@melpomene'; 'gmo@melpomene'; 'Jeff Marr'
Subject: illegal address exceptions
Follow Up Flag: Follow up
Flag Status: Red

Jay Tomlinson wrote (on Fri Sep 30):

Jeff Marr wrote (on Fri Sep 30):

Jay Tomlinson writes:

> Jeff,
>
> You asked me earlier about illegal address exceptions. I looked at the code to
> be sure and as I suspected, this type exception will not prevent a register file
> write and it will not inhibit an NB request.
> The cases covered are:
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> Let me know if you need more information.
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> Jay
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affects?

Thanx,

jeffm

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are not recognized by any of the NB peripherals. This means that there is now 1
less NB entry available.

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intended as a debug aid. That is what gmo said when he request that we change
this from a machine check to an exception. This change was request made so that
SW could find the problem by looking at the exception information.

Whoa! If we need a rest to fix this up then it should be a machine
check not an exception. If it's going to be an exception then we need
to do it right.

Tim

From: Tim B. Robinson [tbr@aphrodite]
Sent: Friday, September 30, 1994 11:15 AM
To: 'Jay Tomlinson'
Cc: 'euterpe@melpomene'; 'gmo@melpomene'; 'Jeff Marr'
Subject: illegal address exceptions

Jay Tomlinson wrote (on Fri Sep 30):

Jeff Marr wrote (on Fri Sep 30):

Jay Tomlinson writes:

> Jeff,

>

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> be sure and as I suspected, this type exception will not prevent a register file
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> The cases covered are:

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> pa[63:48] ~= 0

> pa[47] & not (one of the on-chip resources listed in the memory

map)

>

> Let me know if you need more information.

>

> Jay

What is going to happen when the NB request completes? What are the side
affects?

Thankx,

jeffm

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are not recognized by any of the NB peripherals. This means that there is now 1
less NB entry available.

The assumption here is that a reset must be done after this exception.

This is

intended as a debug aid. That is what gmo said when he request that we change
this from a machine check to an exception. This change was request made so that
SW could find the problem by looking at the exception information.

Whoa! If we need a rest to fix this up then it should be a machine check not an
exception. If it's going to be an exception then we need to do it right.

Tim

From: Geert Rosseel [geert@rhea]
Sent: Friday, September 30, 1994 11:19 AM
To: 'geert@rhea'
Subject: pager log message

page from geert to geert:

pageme gmake geert_euterpegards start:Sep_30_07:57 end: Sep_30_09:16 exit

1

From: Alan Corry [agc@luckboy]
Sent: Friday, September 30, 1994 11:20 AM
To: 'Dave Van't Hof'
Cc: 'Geert Rosseel'
Subject: output of euterpe/verilog/bsrc/dr/.checkoutrc (fwd)

Can you look into this ? TOPT stopped the run with an Exit Code 3, "invalid input data "

Forwarded message:

> From chip@gamorra Fri Sep 30 09:14:56 1994
> Date: Fri, 30 Sep 1994 09:14:56 -0700
> From: chip@gamorra (Buffalo Chip)
> Message-Id: <199409301614.JAA02543@gamorra.microunity.com>
> To: agc@gamorra
> Subject: output of euterpe/verilog/bsrc/dr/.checkoutrc
>
> The output from euterpe/verilog/bsrc/dr/.checkoutrc is 392k, so it is
not included
> in this mail message. Instead, check the file
>
> /n/tmp/chiplog/agc.gamorra.26337.euterpe-verilog-bsrc-dr
>
> (which is accessible from all machines). This file will disappear in
> about 5 days.
>
> By the way, the exit status returned by .checkoutrc was 1.
>

From: sysadm@gaea on behalf of Jeff Marr [jeffm@microunity.com]
Sent: Friday, September 30, 1994 11:30 AM
To: 'euterpe@gaea'

In article <199409292305.QAA15547@aphrodite.microunity.com>, tbr@aphrodite.microunity.com (Tim B. Robinson) writes:

```
>
> We have run into a problem with the GTLB mask field. When the LTLB
> was changed to implement only the XOR field, craig wanted the sense
> of the mask field inverting so that the LTLB mask would be read only
> with a value of 0 rather than all 1's. To be consistent with this,
> the GTLB definition was to be changed too, with the thinking being
> that all we had to do was reverse the sense of the data going in and
> out via the CMOS read/write ports. However, the GTLB physical array
> uses the same I/O pins for the mask and match arrays, effectively
> selecting between them with an additional address bit. So we cannot
> invert one without inverting the other unless we add more logic which
> we can ill afford in order to invert the data selectively.
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> I therefore propose that we go back to the original (and less
> confusing) definition, with the LTLB match field reading back always
> all 1's and no extra inversions in the GTLB path. I think this can
> still be justified as consistent with the general definition of
> reserved fields always reading zero, because this is not really a
> reserved field. It is the LTLB match field, which in this
> implementation happens to have a reserved *value* of all 1's which
> you can't change.
>
> Comments please - and remember atoms are at stake!
>
> Tim
>
```

This is good for verification, since it is more straightforward - which should reduce the number of bugs in the tests, and make debug easier. It also results in a slight reduction in the number of instructions needed to build up the

masks.

--
Jeff "Won't you be my 'lectronic neighbor?" Marr

From: vant [vanthof@hestia]
Sent: Friday, September 30, 1994 11:32 AM
To: 'Alan Corry'
Cc: 'vanthof@luckboy'; 'geert@luckboy'
Subject: Re: output of euterpe/verilog/bsrc/dr/.checkoutrc (fwd)

Alan Corry writes:

```
>  
>Can you look into this ? TOPT stopped the run with an Exit Code 3,  
"invalid  
>input data "
```

There are no intrinsic delays for the new large xor gates and topt doesn't like that. For example:

```
IntrinsicDelayByName: ERROR! cell xbor6df32s missing intrinsic flipflop delay entries for  
fanin 16
```

which gives the Exit code of 3.

The timing numbers need to be updated...

Thanks,
Dave

--

Dave Van't Hof vanthof@microunity.com MicroUnity Systems Engineering,
Inc.

"What rolls down stairs, alone or in pairs, rolls over the neighbor's dog?"

What's great for a snack and fits on your back? It's log, log, log!"

LOG from BLAMMO! (tm) All kids love Log! #include

<std_disclaim.h>

From: Buffalo Chip [chip@rhea]
Sent: Friday, September 30, 1994 11:47 AM
To: 'geert@rhea'
Subject: pager log message

page from chip to geert:

Release euterpe/verilog/bsrc/nb BOM 58.0 initiated by agc completed @ Fri Sep 30 09:45:29
PDT 1994 with exit status 1.. chip

From: lisa
Sent: Friday, September 30, 1994 12:55 PM
To: 'software-checkins-dist'
Subject: gnu-tools/sim/terp trace_types.h

Update of /p/cvsroot/gnu-tools/sim/terp
In directory calliope:/N/hyperion/root/s1/lisa/gnu-tools/sim/terp

Modified Files:
 trace_types.h
Log Message:

Added another trace type: stalls-with-an-address.

From: lisa
Sent: Friday, September 30, 1994 1:07 PM
To: 'software-checkins-dist'
Subject: gnu-tools/include/opcode terp.h

Update of /p/cvsroot/gnu-tools/include/opcode
In directory calliope:/N/hyperion/root/sl/lisa/gnu-tools/include/opcode

Modified Files:
 terp.h

Log Message:

- Added new instruction class IC_SWAP (for cas, mas, etc.).
- Removed some unused instruction types.

From: lisa
Sent: Friday, September 30, 1994 1:09 PM
To: 'software-checkins-dist'
Subject: gnu-tools/opcodes terp-opc.c

Update of /p/cvsroot/gnu-tools/opcodes
In directory calliope:/N/hyperion/root/s1/lisa/gnu-tools/opcodes

Modified Files:
 terp-opc.c
Log Message:

Re-classified the swap instructions (cas, mas, etc.).

From: lisa
Sent: Friday, September 30, 1994 1:10 PM
To: 'software-checkins-dist'
Subject: gnu-tools/sim/terp terp.h

Update of /p/cvsroot/gnu-tools/sim/terp
In directory calliope:/N/hyperion/root/s1/lisa/gnu-tools/sim/terp

Modified Files:

terp.h

Log Message:

- Added some major-to-minor and vice-versa macros.
- Define a generic HICCUP here (9 major cycles).

From: lisa
Sent: Friday, September 30, 1994 1:11 PM
To: 'software-checkins-dist'
Subject: gnu-tools/sim/terp decode.c

Update of /p/cvsroot/gnu-tools/sim/terp
In directory calliope:/N/hyperion/root/sl/lisa/gnu-tools/sim/terp

Modified Files:
 decode.c

Log Message:

Removed instruction types no longer used (previous only for swap insns).

From: lisa
Sent: Friday, September 30, 1994 1:11 PM
To: 'software-checkins-dist'
Subject: gnu-tools/sim/terp execute.h

Update of /p/cvsroot/gnu-tools/sim/terp
In directory calliope:/N/hyperion/root/s1/lisa/gnu-tools/sim/terp

Modified Files:
 execute.h

Log Message:

Define STORE_DATA, etc., macros here (rather than in load_store.c).

From: lisa
Sent: Friday, September 30, 1994 1:13 PM
To: 'software-checkins-dist'
Subject: gnu-tools/sim/terp load_store.c

Update of /p/cvsroot/gnu-tools/sim/terp
In directory calliope:/N/hyperion/root/sl/lisa/gnu-tools/sim/terp

Modified Files:
load_store.c

Log Message:

Clean-up and simplify the swap instructions.

From: lisa
Sent: Friday, September 30, 1994 1:14 PM
To: 'software-checkins-dist'
Subject: gnu-tools/sim/terp cycles.h

Update of /p/cvsroot/gnu-tools/sim/terp
In directory calliope:/N/hyperion/root/s1/lisa/gnu-tools/sim/terp

Modified Files:
 cycles.h
Log Message:

Added new stall type (HSTALL for store-to-load hazards).
Added new trace record macro for stalls-with-address.

From: lisa
Sent: Friday, September 30, 1994 1:14 PM
To: 'software-checkins-dist'
Subject: gnu-tools/sim/terp events.c

Update of /p/cvsroot/gnu-tools/sim/terp
In directory calliope:/N/hyperion/root/sl/lisa/gnu-tools/sim/terp

Modified Files:
events.c

Log Message:

Can now use HICCUP rather than hardwired 9.

From: lisa
Sent: Friday, September 30, 1994 1:15 PM
To: 'software-checkins-dist'
Subject: gnu-tools/sim/terp cycles.c

Update of /p/cvsroot/gnu-tools/sim/terp
In directory calliope:/N/hyperion/root/sl/lisa/gnu-tools/sim/terp

Modified Files:
 cycles.c
Log Message:

New instruction class IC_SWAP (aka 'w').

From: lisa
Sent: Friday, September 30, 1994 1:15 PM
To: 'software-checkins-dist'
Subject: gnu-tools/sim/terp memory.h

Update of /p/cvsroot/gnu-tools/sim/terp
In directory calliope:/N/hyperion/root/sl/lisa/gnu-tools/sim/terp

Modified Files:

memory.h

Log Message:

Implementation of sram hazard detection.

From: lisa
Sent: Friday, September 30, 1994 1:17 PM
To: 'software-checkins-dist'
Subject: gnu-tools/sim/terp execloop.c

Update of /p/cvsroot/gnu-tools/sim/terp
In directory calliope:/N/hyperion/root/s1/lisa/gnu-tools/sim/terp

Modified Files:
 execloop.c

Log Message:

- In data_access_cache(): record store's and check for hazardous loads.
- Handle the store-data register dependencies of instructions of class IC_SWAP similarly to those of IC_STORE.

From: lisa
Sent: Friday, September 30, 1994 1:18 PM
To: 'software-checkins-dist'
Subject: gnu-tools/sim/terp memory.c

Update of /p/cvsroot/gnu-tools/sim/terp
In directory calliope:/N/hyperion/root/sl/lisa/gnu-tools/sim/terp

Modified Files:
memory.c

Log Message:

- Implementation of sram hazard detection.
- NB_HICCUP definition removed; changed all NB_HICCUPS to HICCUPS.

From: vant [vanthof@hestia]
Sent: Friday, September 30, 1994 1:19 PM
To: 'Tom Vo'; 'Geert Rosseel'
Cc: 'Dave Van't Hof'; 'Mark Hofmann'; 'Tim B. Robinson'; 'Lisa Robinson'
Subject: lvs mismatches in xbc01df4s?

Hi, I believe I've found one reason why the fullchip euterpe lvs didn't work. The XBC01DF4S cell does not pass LVS. There are several devices missing from the layout:

NUMBER OF UN-MATCHED SCHEMATICS DEVICES	=	5
NUMBER OF UN-MATCHED LAYOUT DEVICES	=	2
NUMBER OF MATCHED SCHEMATICS DEVICES	=	1
NUMBER OF MATCHED LAYOUT DEVICES	=	1

I heard hallway talk about the C01 cells being regenerated, is this one of

the repercussions? I guess the leaf cells need to be regenerated? Until they are, there is not a very good reason for running fullchip lvs's.

Thanks,
Dave

--
Dave Van't Hof vanthof@microunity.com MicroUnity Systems Engineering,
Inc.
"What rolls down stairs, alone or in pairs, rolls over the neighbor's dog?"

What's great for a snack and fits on your back? It's log, log, log!"
LOG from BLAMMO! (tm) All kids love Log! #include
<std_disclaim.h>

From: lisa
Sent: Friday, September 30, 1994 1:19 PM
To: 'software-checkins-dist'
Subject: gnu-tools/sim/terp stats.c

Update of /p/cvsroot/gnu-tools/sim/terp
In directory calliope:/N/hyperion/root/s1/lisa/gnu-tools/sim/terp

Modified Files:
stats.c

Log Message:

- Print stalls due to store-to-load hazard hiccups.
- Print statistics of sram hazard detection at the various granularities.

From: Buffalo Chip [chip@ghidra]
Sent: Friday, September 30, 1994 2:29 PM
To: 'geert@ghidra'
Subject: output of euterpe/verilog/bsrc/ctio/.checkoutrc

Fri Sep 30 12:25:04 PDT 1994 (geert Fri, 30 Sep 1994 12:24:41 -0700)
euterpe/verilog/bsrc/ctio
[Release BOM (V18.0) in euterpe/verilog/bsrc/ctio (Fri Sep 30 12:25:04 PDT 1994)]

Dir euterpe/verilog/bsrc/ctio BOM 18.0

7.3 .checkoutrc
1.8 Makefile
10.2 clean-request
1.3 ctio.V
3.1 ctio.ut
11.2 ctio1_control.pim
(11.1)
3.1 ctiotester.V
3.1 ctiotester.h
1.2 ctrasel.pla
3.1 ctwasel.pla
3.1 ctwe.Veqn
9.3 genpim0.pl
9.3 genpim1.pl
13.5 genptab.pl
5.8 pimlib.pl (5.7)

==> running euterpe/verilog/bsrc/ctio/.checkoutrc (Fri Sep 30 12:25:13 PDT 1994) <===

gmake: 'clean' is up to date.

cat: write error: No space left on device

** SLNET 1.037 ** SL_NET V1.000 -- Netlist Manipulator Copyright (c) 1993,1994 SILVAR-
LISCO. All rights reserved.

Design: ctio0-pass1 Started at: 94/09/30 12:28:53

Loading file "ctio0-pass1.sdl".

[XBFFDF6S]
[XBFFBDH12S]
[XBFFDH4S]
[XBFFDH2S]
[XBFFDF4S]
[XBFFBDF6S]
[XBORFF2DF4S]
[XBORFFB2DH12S]
[XBORFF2DH4S]
[XBMUXFF3DH24S]
[XBMUXFF2DF24S]
[XBMUXFF2DH4S]
[XBOR2DF24S]
[XBOR3DF24S]
[XBORFF3DF8S]
[XBORFF4DF24S]
[CGCLOCKBIAS]
[CTIO]

** Warning: No nets connected to component CGCLOCKBIAS.

Translating...

[XBFFDF6S]
[XBFFBDH12S]
[XBFFDH4S]
[XBFFDH2S]
[XBFFDF4S]
[XBFFBDF6S]
[XBORFF2DF4S]

```

[XBORFFB2DH12S]
[XBORFF2DH4S]
[XBMUXFF3DH24S]
[XBMUXFF2DF24S]
[XBMUXFF2DH4S]
[XBOR2DF24S]
[XBOR3DF24S]
[XBORFF3DF8S]
[XBORFF4DF24S]
[CGCLOCKBIAS]
[CTIO]

```

Netlist Info :

```

Number of logic types      : 17
Number of nets             : 704
Number of components       : 180
Number of component pins   : 2078
Number of pins/comp        : 11.544444
Number of nets/comp        : 3.911111

```

Size estimation :

size	TYPE	# inst	size/inst	total
+-----+-----+-----+-----+				
	XBORFF3DF8S	8	1	8
	XBFFBDF6S	1	1	1
	XBFFDF6S	1	1	1
	XBORFFB2DH12S	2	1	2
	XBMUXFF2DH4S	64	1	64
	XBFFDF4S	7	1	7
	XBMUXFF3DH24S	16	1	16
	CGCLOCKBIAS	1	1	1
	XBOR3DF24S	1	1	1
	XBMUXFF2DF24S	64	1	64
	XBORFF4DF24S	1	1	1
	XBOR2DF24S	4	1	4
	XBORFF2DF4S	1	1	1
	XBORFF2DH4S	4	1	4
	XBFFBDH12S	2	1	2
	XBFFDH4S	2	1	2
	XBFFDH2S	1	1	1
+-----+-----+-----+-----+				
	TOTAL	180	1	180

```

+-----+-----+-----+-----+-----+
Warning : No "SL_SIZE" attributes found on the cells!
Default size (1) was used for all cells.
To change this default add an attribute "SL_SIZE" to the cells.

```

```

Requires a minimum license of gardsfel_3 or gardsl_3 .
Applicable licenses available at your installation :
    gardsconfig_3
Checked out one user token of a gardsconfig_3 license.

```

```

gmake[2]: *** [gards/ctio0-pass1.pcomp.lis] Error 1
gmake[1]: *** [ctio0-base.short.nets] Error 1
gmake: *** [ctio0gards] Error 1
#
# turn off pgroute
#
[ -f gards/nopgroute ] || touch gards/nopgroute # # use padtiles # [ -f gards/usepadtiles
] || touch gards/usepadtiles # # use pifpack # [ -f gards/usepifpack ] || touch
gards/usepifpack # # insert an instance of the clock tree # [ -f gards/addclock ] || touch
gards/addclock # # disable old dcell placement obstruction # [ -f gards/noobs ] || touch
gards/noobs # # now do it . . .
#
gmake GARDS_DISPLAY=clio:0.0 gards/ctio0-iter
gmake[1]: Entering directory
~/N/auspex/root/s10/chip/euterpe/verilog/bsrc/ctio'
cat /n/auspex/s10/chip/euterpe/proteus/verilog/dxlib/xlib.config
/n/auspex/s10/chip/euterpe/proteus/verilog/dclib/clib.config
/n/auspex/s10/chip/euterpe/proteus/verilog/delib/elib.config > gards/ctio0.v2e.config # #
Take a snooze to make sure vfiles looks older than the .v2e file # when they are on
different NFS file systems # sleep 60 CHIPROOT=/n/auspex/s10/chip/euterpe
/n/auspex/s10/chip/euterpe/tools/bin/v2e -host ghidra -f vfiles -o gards/ctio0.v2e -c
gards/ctio0.v2e.config -l gards/ctio0.v2e.log -y
/n/auspex/s10/chip/euterpe/proteus/verilog/mlib+libext+.v -y
/n/auspex/s10/chip/euterpe/proteus/verilog/dxlib -y
/n/auspex/s10/chip/euterpe/proteus/verilog/dclib -y
/n/auspex/s10/chip/euterpe/proteus/verilog/delib
V2E 1.0a Sep 30, 1994 12:26:25
* Copyright Cadence Design Systems Inc. 1990. *
* All Rights Reserved. Licensed Software. *
* Confidential and proprietary information which is the *
* property of Cadence Design Systems Inc. *
Compiling source file "ctio.v"
Compiling source file "ctrasel.v"
Compiling source file "ctwasel.v"
Compiling source file "ctwe.v"
Scanning library directory
"/n/auspex/s10/chip/euterpe/proteus/verilog/mlib"
Scanning library directory
"/n/auspex/s10/chip/euterpe/proteus/verilog/dxlib"
Warning! library directory
"/n/auspex/s10/chip/euterpe/proteus/verilog/dclib" was specified but not needed.
Warning! library directory
"/n/auspex/s10/chip/euterpe/proteus/verilog/delib" was specified but not needed.
Highest level modules:
ctio

Reading configuration file gards/ctio0.v2e.config ....
Processing configuration file ....
Translating Verilog source ....
Writing output to gards/ctio0.v2e ....
0 warnings 0 errors
End of V2E 1.0a Sep 30, 1994 12:26:37
CHIPROOT=/n/auspex/s10/chip/euterpe
/n/auspex/s10/chip/euterpe/tools/bin/emerger -f -R -p gards/ctio0.emerger.tab -e
gards/ctio0.v2e -o gards/ctio0.edif -O gards/ctio0.emerger.log -I ../cg/cgclockbias.v2e

```

cgclockbias

Running emerge compiled on Thu Sep 29 19:59:36 GMT 1994

```
Consuming edif file gards/ctio0.v2e
Found edif structure: CTIO0_46_V2E
Flattening edif;
  Flattened 181 instances;      created 32 nets in CTIO0_46_V2E
Reading Edif file for instance placement: ../cg/cgclockbias.v2e
Consuming power table information file gards/ctio0.emerge.tab
Performing Edif Transformations...
Warning! Port phi_A2P already top level.
Warning! Port phi_B2P already top level.
Disgorging edif file gards/ctio0.edif
Writing edif structure: gards_47_ctio0_46_edif Memory usage: 1.629MB
/usr/local/bin/perl genpim0.pl > pim.tmp mv pim.tmp gards/ctio0-pass1.pim # # Get an
initial sdl file. A manhattan approximation will be used # gmake GARDS_DISPLAY=clio:0.0
CYCLETIME=895 gards/ctio0-pass2.sdl
gmake[2]: Entering directory
~/N/auspex/root/s10/chip/euterpe/verilog/bsrc/ctio'
CHIPROOT=/n/auspex/s10/chip/euterpe
/n/auspex/s10/chip/euterpe/tools/bin/topt -p
/n/auspex/s10/chip/euterpe/proteus/misc/power.tab -p gards/ctio0.power.tab.local \
-h /n/auspex/s10/chip/euterpe/proteus/leafgen/dclload/dclload.lib -h
/n/auspex/s10/chip/euterpe/proteus/exlax/dclload/dclload.lib -h
/n/auspex/s10/chip/euterpe/proteus/custom/dclload/dclload.lib \
-g /n/auspex/s10/chip/euterpe/proteus/leafgen/toptList -g
/n/auspex/s10/chip/euterpe/proteus/exlax/toptList -g
/n/auspex/s10/chip/euterpe/proteus/custom/toptList \
-A /n/auspex/s10/chip/euterpe/proteus/leafgen/caps/cap.lib -A
/n/auspex/s10/chip/euterpe/proteus/exlax/caps/cap.lib -A
/n/auspex/s10/chip/euterpe/proteus/custom/caps/cap.lib \
-H /n/auspex/s10/chip/euterpe/proteus/leafgen/time/tim.lib -H
/n/auspex/s10/chip/euterpe/proteus/custom/time/tim.lib -H
/n/auspex/s10/chip/euterpe/proteus/exlax/time/tim.lib \
-l 895 \
-e gards/ctio0.edif \
-k gards/ctio0-pass1.strength \
-B gards/ctio0-pass1.sdl \
-s gards/ctio0-pass1.stat \
-O gards/ctio0-pass1.topt.log \
-z 2 -M mobimos -R -t 50 -b 10 -a 24 -0 -F
```

Running topt (Timing OPTimizer) compiled on Thu Sep 29 23:13:10 GMT 1994

```
Processing a: Mobimos, Flop/Latch design
Consuming edif file gards/ctio0.edif
Found edif structure: gards_47_ctio0_46_edif
Flattening edif;
  CTIO already flat.
  found 182 instances;      found 730 nets in gards_47_ctio0_46_edif
Consuming power table information file
/n/auspex/s10/chip/euterpe/proteus/misc/power.tab
Consuming power table information file gards/ctio0.power.tab.local
Reading Stats file
/n/auspex/s10/chip/euterpe/proteus/leafgen/stats.ec1
Reading Stats file
/n/auspex/s10/chip/euterpe/proteus/leafgen/stats.cmos
Reading Stats file /n/auspex/s10/chip/euterpe/proteus/exlax/stats.ea
Reading Stats file
/n/auspex/s10/chip/euterpe/proteus/custom/stats.ec1
Reading Legal Cell List file
/n/auspex/s10/chip/euterpe/proteus/leafgen/toptList
Reading Legal Cell List file
/n/auspex/s10/chip/euterpe/proteus/exlax/toptList
Reading Legal Cell List file
/n/auspex/s10/chip/euterpe/proteus/custom/toptList
Performing Edif Transformations...
```



```

    Reading DC Loads file
/n/auspex/s10/chip/euterpe/proteus/leafgen/dclload/dclload.lib
    Reading DC Loads file
/n/auspex/s10/chip/euterpe/proteus/exlax/dclload/dclload.lib
    Reading DC Loads file
/n/auspex/s10/chip/euterpe/proteus/custom/dclload/dclload.lib

    Reading pin cap values from
/n/auspex/s10/chip/euterpe/proteus/leafgen/caps/cap.lib
    Reading pin cap values from
/n/auspex/s10/chip/euterpe/proteus/exlax/caps/cap.lib
    Reading pin cap values from
/n/auspex/s10/chip/euterpe/proteus/custom/caps/cap.lib
    Status information in gards/ctio0-pass1.stat Warning! Cell cgclockbias not on legal
cell list.
    Any gate in it's path is not AC power optimized
    No swing calculations will be performed
    Pruning flattened network of unused instances... 2 pruned in 2
passes.
    Checking/Setting swing values...

    Reading Cap/Delay table file
/n/auspex/s10/chip/euterpe/proteus/leafgen/time/tim.lib
    Reading Cap/Delay table file
/n/auspex/s10/chip/euterpe/proteus/custom/time/tim.lib
Warning! Cell cache at line 4 is not in legal cell list Warning! Cell cahalf at line 10
is not in legal cell list Warning! Cell cr at line 13 is not in legal cell list Warning!
Cell ctg at line 20 is not in legal cell list Warning! Cell gt1b at line 23 is not in
legal cell list Warning! Cell sccgbr0 at line 52 is not in legal cell list Warning!
Cell sccgdr at line 94 is not in legal cell list
    Reading Cap/Delay table file
/n/auspex/s10/chip/euterpe/proteus/exlax/time/tim.lib

    Connecting floating differential inputs to net vref_0ph...
    Connected 0 inputs to net vref_0ph...
    DC Load checks only for cell(s):
eawwlvref56s7x4a eawwlvref20s10x1a eawwlvref16s2x4a xbc01df32s
xbc01df24s xbc01df16s xbc01df12s xbc01df8s xbc01df6s xbc01df4s
xbc01df2s xbc01 xbcmos2ecldf16s xbcmos2ecldf12s xbcmos2ecldf8s
xbcmos2ecldf4s xbcmos2ecldf2s xbcmos2ecldf1s
    Force swing levels for inst(s):
ctwe/UCTweB7/u0;(df) ctwe/UCTweB6/u0;(df) ctwe/UCTweB5/u0;(df)
ctwe/UCTweB4/u0;(df)
ctwe/UCTweB3/u0;(df) ctwe/UCTweB2/u0;(df) ctwe/UCTweB1/u0;(df)
ctwe/UCTweB0/u0;(df)
muxff2_32dinhi/u0;(df) muxff2_32dinhi/u1;(df)
muxff2_32dinhi/u2;(df)
muxff2_32dinhi/u3;(df) muxff2_32dinhi/u4;(df)
muxff2_32dinhi/u5;(df)
muxff2_32dinhi/u6;(df) muxff2_32dinhi/u7;(df)
muxff2_32dinhi/u8;(df)
muxff2_32dinhi/u9;(df) muxff2_32dinhi/u10;(df)
muxff2_32dinhi/u11;(df)
muxff2_32dinhi/u12;(df) muxff2_32dinhi/u13;(df)
muxff2_32dinhi/u14;(df)
muxff2_32dinhi/u15;(df) muxff2_32dinhi/u16;(df)
muxff2_32dinhi/u17;(df)
muxff2_32dinhi/u18;(df) muxff2_32dinhi/u19;(df)
muxff2_32dinhi/u20;(df)
muxff2_32dinhi/u21;(df) muxff2_32dinhi/u22;(df)
muxff2_32dinhi/u23;(df)
muxff2_32dinhi/u24;(df) muxff2_32dinhi/u25;(df)
muxff2_32dinhi/u26;(df)
muxff2_32dinhi/u27;(df) muxff2_32dinhi/u28;(df)
muxff2_32dinhi/u29;(df)
muxff2_32dinhi/u30;(df) muxff2_32dinhi/u31;(df)
muxff2_32dinlo/u0;(df)
muxff2_32dinlo/u1;(df) muxff2_32dinlo/u2;(df)

```

```

muxfff2_32dinlo/u3; (df)
muxfff2_32dinlo/u4; (df) muxfff2_32dinlo/u5; (df)
muxfff2_32dinlo/u6; (df)
muxfff2_32dinlo/u7; (df) muxfff2_32dinlo/u8; (df)
muxfff2_32dinlo/u9; (df)
muxfff2_32dinlo/u10; (df) muxfff2_32dinlo/u11; (df)
muxfff2_32dinlo/u12; (df)
muxfff2_32dinlo/u13; (df) muxfff2_32dinlo/u14; (df)
muxfff2_32dinlo/u15; (df)
muxfff2_32dinlo/u16; (df) muxfff2_32dinlo/u17; (df)
muxfff2_32dinlo/u18; (df)
muxfff2_32dinlo/u19; (df) muxfff2_32dinlo/u20; (df)
muxfff2_32dinlo/u21; (df)
muxfff2_32dinlo/u22; (df) muxfff2_32dinlo/u23; (df)
muxfff2_32dinlo/u24; (df)
muxfff2_32dinlo/u25; (df) muxfff2_32dinlo/u26; (df)
muxfff2_32dinlo/u27; (df)
muxfff2_32dinlo/u28; (df) muxfff2_32dinlo/u29; (df)
muxfff2_32dinlo/u30; (df)
muxfff2_32dinlo/u31; (df) muxfff2_32douthi/u0; (dh)
muxfff2_32douthi/u1; (dh)
muxfff2_32douthi/u2; (dh) muxfff2_32douthi/u3; (dh)
muxfff2_32douthi/u4; (dh)
muxfff2_32douthi/u5; (dh) muxfff2_32douthi/u6; (dh)
muxfff2_32douthi/u7; (dh)
muxfff2_32douthi/u8; (dh) muxfff2_32douthi/u9; (dh)
muxfff2_32douthi/u10; (dh)
muxfff2_32douthi/u11; (dh) muxfff2_32douthi/u12; (dh)
muxfff2_32douthi/u13; (dh)
muxfff2_32douthi/u14; (dh) muxfff2_32douthi/u15; (dh)
muxfff2_32douthi/u16; (dh)
muxfff2_32douthi/u17; (dh) muxfff2_32douthi/u18; (dh)
muxfff2_32douthi/u19; (dh)
muxfff2_32douthi/u20; (dh) muxfff2_32douthi/u21; (dh)
muxfff2_32douthi/u22; (dh)
muxfff2_32douthi/u23; (dh) muxfff2_32douthi/u24; (dh)
muxfff2_32douthi/u25; (dh)
muxfff2_32douthi/u26; (dh) muxfff2_32douthi/u27; (dh)
muxfff2_32douthi/u28; (dh)
muxfff2_32douthi/u29; (dh) muxfff2_32douthi/u30; (dh)
muxfff2_32douthi/u31; (dh)
muxfff2_32doutlo/u0; (dh) muxfff2_32doutlo/u1; (dh)
muxfff2_32doutlo/u2; (dh)
muxfff2_32doutlo/u3; (dh) muxfff2_32doutlo/u4; (dh)
muxfff2_32doutlo/u5; (dh)
muxfff2_32doutlo/u6; (dh) muxfff2_32doutlo/u7; (dh)
muxfff2_32doutlo/u8; (dh)
muxfff2_32doutlo/u9; (dh) muxfff2_32doutlo/u10; (dh)
muxfff2_32doutlo/u11; (dh)
muxfff2_32doutlo/u12; (dh) muxfff2_32doutlo/u13; (dh)
muxfff2_32doutlo/u14; (dh)
muxfff2_32doutlo/u15; (dh) muxfff2_32doutlo/u16; (dh)
muxfff2_32doutlo/u17; (dh)
muxfff2_32doutlo/u18; (dh) muxfff2_32doutlo/u19; (dh)
muxfff2_32doutlo/u20; (dh)
muxfff2_32doutlo/u21; (dh) muxfff2_32doutlo/u22; (dh)
muxfff2_32doutlo/u23; (dh)
muxfff2_32doutlo/u24; (dh) muxfff2_32doutlo/u25; (dh)
muxfff2_32doutlo/u26; (dh)
muxfff2_32doutlo/u27; (dh) muxfff2_32doutlo/u28; (dh)
muxfff2_32doutlo/u29; (dh)
muxfff2_32doutlo/u30; (dh) muxfff2_32doutlo/u31; (dh) Warning! No CKFI_AD1PH pin
capacitance data for cgclockbias Warning! No CKFI_BD1PH pin capacitance data for
cgclockbias Warning! No CKRI_AD1PH pin capacitance data for cgclockbias Warning! No
CKRI_BD1PH pin capacitance data for cgclockbias Warning! No CLR_ABM<8> pin capacitance
data for cgclockbias Warning! No CLR_ABM<7> pin capacitance data for cgclockbias Warning!
No CLR_ABM<6> pin capacitance data for cgclockbias Warning! No CLR_ABM<5> pin capacitance
data for cgclockbias Warning! No CLR_ABM<4> pin capacitance data for cgclockbias Warning!

```

No CLR_ABM<3> pin capacitance data for cgclockbias Warning! No CLR_ABM<2> pin capacitance data for cgclockbias Warning!
 No CLR_ABM<0> pin capacitance data for cgclockbias Warning! No CLR_ABM<1> pin capacitance data for cgclockbias Warning!
 data for cgclockbias Warning! No PHI_ANM<7> pin capacitance data for cgclockbias Warning!
 No PHI_ANM<6> pin capacitance data for cgclockbias Warning! No PHI_ANM<4> pin capacitance data for cgclockbias Warning!
 data for cgclockbias Warning! No PHI_ANM<3> pin capacitance data for cgclockbias Warning!
 data for cgclockbias Warning! No PHI_ANM<1> pin capacitance data for cgclockbias Warning!
 No PHI_ANM<0> pin capacitance data for cgclockbias Warning! No PHI_BNM<7> pin capacitance data for cgclockbias Warning!
 data for cgclockbias Warning! No PHI_BNM<6> pin capacitance data for cgclockbias Warning!
 data for cgclockbias Warning! No PHI_BNM<4> pin capacitance data for cgclockbias Warning!
 No PHI_BNM<3> pin capacitance data for cgclockbias Warning! No PHI_BNM<5> pin capacitance data for cgclockbias Warning!
 data for cgclockbias Warning! No PHI_BNM<2> pin capacitance data for cgclockbias Warning!
 No PHI_BNM<0> pin capacitance data for cgclockbias Warning! No RD_BM<8> pin capacitance data for cgclockbias Warning!
 data for cgclockbias Warning! No RD_BM<7> pin capacitance data for cgclockbias Warning!
 No RD_BM<6> pin capacitance data for cgclockbias Warning! No RD_BM<5> pin capacitance data for cgclockbias Warning!
 data for cgclockbias Warning! No RD_BM<4> pin capacitance data for cgclockbias Warning!
 No RD_BM<3> pin capacitance data for cgclockbias Warning! No RD_BM<2> pin capacitance data for cgclockbias Warning!
 data for cgclockbias Warning! No RD_BM<1> pin capacitance data for cgclockbias Warning!
 No RD_BM<0> pin capacitance data for cgclockbias Warning! No SI_AM<8> pin capacitance data for cgclockbias Warning!
 data for cgclockbias Warning! No SI_AM<7> pin capacitance data for cgclockbias Warning!
 No SI_AM<6> pin capacitance data for cgclockbias Warning! No SI_AM<5> pin capacitance data for cgclockbias Warning!
 data for cgclockbias Warning! No SI_AM<4> pin capacitance data for cgclockbias Warning!
 No SI_AM<3> pin capacitance data for cgclockbias Warning! No SI_AM<2> pin capacitance data for cgclockbias Warning!
 data for cgclockbias Warning! No SI_AM<1> pin capacitance data for cgclockbias Warning!
 No SI_AM<0> pin capacitance data for cgclockbias Warning! No VFFMAX pin capacitance data for cgclockbias Warning!
 No VFFMIN pin capacitance data for cgclockbias Warning! No VFFREFMAX pin capacitance data for cgclockbias Warning!
 No VFFREFMIN pin capacitance data for cgclockbias Warning! No VFFREFVAR pin capacitance data for cgclockbias Warning!
 No VFFVAR pin capacitance data for cgclockbias Warning! No VRRG<2> pin capacitance data for cgclockbias Warning!
 No VRRG<1> pin capacitance data for cgclockbias Warning!
 No VRRG<0> pin capacitance data for cgclockbias Warning! No XFER_BM<8> pin capacitance data for cgclockbias Warning!
 No XFER_BM<7> pin capacitance data for cgclockbias Warning!
 No XFER_BM<6> pin capacitance data for cgclockbias Warning!
 No XFER_BM<5> pin capacitance data for cgclockbias Warning!
 No XFER_BM<4> pin capacitance data for cgclockbias Warning!
 No XFER_BM<3> pin capacitance data for cgclockbias Warning!
 No XFER_BM<2> pin capacitance data for cgclockbias Warning!
 No XFER_BM<1> pin capacitance data for cgclockbias Warning!
 No XFER_BM<0> pin capacitance data for cgclockbias

Ignoring these nets:
 phi_B2P phi_A2P vref_0ph

Optimizing power...

Iteration: 1
 Path power optimizer
 DC Load Calculations
 Unpowered Instance check: 1 found.
 Iteration: 2
 Path power optimizer
 DC Load Calculations
 Unpowered Instance check: 1 found.

Squeezing out extra time in paths.

Iteration: 3
 Path power optimizer
 DC Load Calculations
 Unpowered Instance check: 1 found.

Savings by squeezing out extra time = (2502 - 2502) = 0.00% Change from original input
 power = (2502 - 320) = 87.21%

Warning! 1 unpowered or untouched instances.

NOTE: 574 unpowered nets.

NOTE: 84 nets with delays less than 50.00ps

NOTE: Power levels changed for 107 instances.

Atoms:	count	atom	bjt	isrc	pld	clock
BJT Totals:	180	2752	4745	4612	3970	2820

Generating instance drive strength file gards/ctio0-pass1.strength
Disgorging sdl file gards/ctio0-pass1.sdl
Writing sdl structure: gards_47_ctio0_46_edif

Congratulations! No timing or DC Load violations!

```
Memory usage: 23.625MB
Exit code: 0 (Success)
CHIPROOT=/n/auspex/s10/chip/euterpe
/n/auspex/s10/chip/euterpe/tools/bin/pdcat -p
/n/auspex/s10/chip/euterpe/clockbias:/n/auspex/s10/chip/euterpe/gards/subb
locks:/n/auspex/s10/chip/euterpe/gards/dcell:/n/auspex/s10/chip/euterpe/pr
oteus/gards/leaf:/n/auspex/s10/chip/euterpe/teus/gards/sofa:/n/auspex/s
10/chip/euterpe/teus/gards/dcell `grep -v '^#' < gards/ctio0-pass1.strength | awk
{'print $4;}' | \
    sort | uniq | awk {'printf ("%s.pdl ", $1)}'` > gards/ctio0-pass1.macros.temp mv
gards/ctio0-pass1.macros.temp gards/ctio0-pass1macros.pdl
**** SLNET ctio0-pass1
Fri Sep 30 12:28:50 PDT 1994
sed -e 's!DESIGN_NAME!ctio0-pass1!' -e "s!EDIF_FILE!ctio0-pass1.sdl!" \
    -e 's!CHIPROOT!/n/auspex/s10/chip/euterpe!' -e 's!TECH_GPLACE!ctio0-
pass1.gplace.mobi234!'\
    -e 's!TECH_REEDIT!ctio0-pass1.reedit.mobi234!'\ \
    < /n/auspex/s10/chip/euterpe/teus/misc/gards.vrf > gards/ctio0-pass1.vrf echo "cd
`abspath`/gards; \
    echo translate_all | HOME=/n/auspex/s10/chip/euterpe/tools
LM_LICENSE_FILE=/n/auspex/s10/chip/euterpe/tools/s1/license/license.dat
DISPLAY=clio:0.0 SL TOTAL_DURATION=500 CHIPROOT=/n/auspex/s10/chip/euterpe
/n/auspex/s10/chip/euterpe/tools/s1/net/dir/slnet ctio0-pass1" | /usr/local/bin/rexec
ghidra sh slnet > 12:28:58 Terminating Normally on 94/09/30
Elapsed CPU time 00:00:04
Elapsed wall time 00:00:05
End of Program
```

Normal Termination ...

```
Fri Sep 30 12:28:58 PDT 1994
**** PCOMP ctio0-pass1
Fri Sep 30 12:28:59 PDT 1994
sed -e 's!DESIGN_NAME!ctio0-pass1!' -e "s!EDIF_FILE!ctio0-pass1.sdl!" \
    -e 's!CHIPROOT!/n/auspex/s10/chip/euterpe!' -e 's!TECH_GPLACE!ctio0-
pass1.gplace.mobi234!'\
    -e 's!TECH_REEDIT!ctio0-pass1.reedit.mobi234!'\ \
    < /n/auspex/s10/chip/euterpe/teus/misc/gards.vrf > gards/ctio0-pass1.vrf rm -f
gards/ctio0-pass1.dff (echo "cd `abspath`/gards; \
    HOME=/n/auspex/s10/chip/euterpe/tools
LM_LICENSE_FILE=/n/auspex/s10/chip/euterpe/tools/s1/license/license.dat
DISPLAY=clio:0.0 SL TOTAL_DURATION=500 CHIPROOT=/n/auspex/s10/chip/euterpe
/n/auspex/s10/chip/euterpe/tools/s1/bin/invoke pcomp ctio0-pass1 -listing ctio0-
pass1.pcomp.lis" | /usr/local/bin/rexec ghidra sh && sleep 10 && \
    HOME=/n/auspex/s10/chip/euterpe/tools
LM_LICENSE_FILE=/n/auspex/s10/chip/euterpe/tools/s1/license/license.dat
DISPLAY=clio:0.0 SL TOTAL_DURATION=500 CHIPROOT=/n/auspex/s10/chip/euterpe
/n/auspex/s10/chip/euterpe/tools/bin/gastatus -ds gards/ctio0-pass1 ) || (mv gards/ctio0-
pass1.pcomp.lis gards/ctio0-pass1.pcomp.lis.ERROR; false) GARDS PCOMP 7.121 -- Physical
Compiler Copyright (c) 1994 SILVAR-LISCO. All rights reserved.
Design: ctio0-pass1 Started at: 94/09/30 12:29:06
```

PCOMP Version 7.1.21 of August 9, 1994

Processing Logic description: CTIO

Processing Expansion level: SLNET

... Start of netlist processing.
... Circuit name: CTIO
... Processing CDL.
... CHIPNAME:SOFA;

... Processing header of user PDL.
... PHYSICALLIB:PBUILD;
... Processing header of system PDL.
... PHYSICALLIB:PBUILD;
... Processing rest of user PDL.
... Processing rest of system PDL.
In Physical at line 892:
--> END_OF_FILE;

** Syntax Error: Physical type XBORFFB2DH12S is not found in the physical libraries.
(Message number 6 Severity 5)

** Syntax Error: Physical type XBORFF4DF24S is not found in the physical libraries.
(Message number 6 Severity 5)

** Syntax Error: Physical type XBORFF3DF8S is not found in the physical libraries.
(Message number 6 Severity 5)

** Syntax Error: Physical type XBORFF2DH4S is not found in the physical libraries.
(Message number 6 Severity 5)

** Syntax Error: Physical type XBORFF2DF4S is not found in the physical libraries.
(Message number 6 Severity 5)

** Syntax Error: Physical type XBOR3DF24S is not found in the physical libraries.
(Message number 6 Severity 5)

** Syntax Error: Physical type XBOR2DF24S is not found in the physical libraries.
(Message number 6 Severity 5)

** Syntax Error: Physical type XBMUXFF3DH24S is not found in the physical libraries.
(Message number 6 Severity 5)

** Syntax Error: Physical type XBMUXFF2DH4S is not found in the physical libraries.
(Message number 6 Severity 5)

** Syntax Error: Physical type XBMUXFF2DF24S is not found in the physical libraries.
(Message number 6 Severity 5)

** Syntax Error: Physical type XBFFDH4S is not found in the physical libraries.
(Message number 6 Severity 5)

** Syntax Error: Physical type XBFFDH2S is not found in the physical libraries.
(Message number 6 Severity 5)

** Syntax Error: Physical type XBFFDF6S is not found in the physical libraries.
(Message number 6 Severity 5)

** Syntax Error: Physical type XBFFDF4S is not found in the physical libraries.
(Message number 6 Severity 5)

** Syntax Error: Physical type XBFFBDH12S is not found in the physical libraries.
(Message number 6 Severity 5)

** Syntax Error: Physical type XBFFBDF6S is not found in the physical libraries.
(Message number 6 Severity 5)

** Syntax Error: Physical type CGCLOCKBIAS is not found in the physical libraries.
(Message number 6 Severity 5)

```
... Processing TDL.
... TECHNOLOGYLIB:SOFA;
... Computed Grid_Size = 1000
... Final Processing.
    17 fatal errors occurred. PCOMP aborting.

Terminated at      : 94/09/30 12:29:10
Elapsed CPU time   : 0 Hrs  0 Mins  2 Secs
Elapsed wall clock time : 0 Hrs  0 Mins  4 Secs
gmake[2]: Leaving directory
`/N/auspex/root/s10/chip/euterpe/verilog/bsrc/ctio'
gmake[1]: Leaving directory
`/N/auspex/root/s10/chip/euterpe/verilog/bsrc/ctio'
[finished at Fri Sep 30 12:29:11 PDT 1994 -- exit status 1]
```

.

From: tbr
Sent: Friday, September 30, 1994 3:22 PM
To: 'ericm'
Cc: 'hopper'; 'tom'
Subject: auspex/s40
Follow Up Flag: Follow up
Flag Status: Red

I have moved about 150MB out of s37 into s40. We have still a way to go in getting all the pieces of euterpe built, so we should expect s40 to fill up a lot more before we are done.

Thanks for the instant allocation.

Tim

From: Buffalo Chip [chip@ghidra]
Sent: Friday, September 30, 1994 3:48 PM
To: 'geert@ghidra'
Subject: output of euterpe/verilog/bsrc/ctio/.checkoutrc

The output from euterpe/verilog/bsrc/ctio/.checkoutrc is 160k, so it is not included in this mail message. Instead, check the file

/n/tmp/chiplog/geert.ghidra.24821.euterpe-verilog-bsrc-ctio

(which is accessible from all machines). This file will disappear in about 5 days.

By the way, the exit status returned by .checkoutrc was 1.

From: Buffalo Chip [chip@ghidra]
Sent: Friday, September 30, 1994 4:09 PM
To: 'geert@ghidra'
Subject: 'output of euterpe/verilog/bsrc/ctio/.checkoutrc

Fri Sep 30 14:08:13 PDT 1994 (geert Fri, 30 Sep 1994 14:08:04 -0700)
euterpe/verilog/bsrc/ctio
[Release BOM (V19.0) in euterpe/verilog/bsrc/ctio (Fri Sep 30 14:08:13 PDT 1994)]

Dir euterpe/verilog/bsrc/ctio BOM 19.0

7.3 .checkoutrc
1.8 Makefile
10.3 clean-request
1.3 ctio.V
3.1 ctio.ut
11.2 ctio1_control.pim
3.1 ctiotester.V
3.1 ctiotester.h
1.2 ctrasel.pla
3.1 ctwasel.pla
3.1 ctwe.Veqn
9.3 genpim0.pl
9.3 genpim1.pl
13.5 genptab.pl
5.8 pimlib.pl

==> running euterpe/verilog/bsrc/ctio/.checkoutrc (Fri Sep 30 14:08:19 PDT 1994) <==

gmake: `clean' is up to date.

gmake[2]: *** No rule to make target `gards/ctio1-pass2.sdl'. Stop.

gmake[1]: *** [ctio1-base.netcap] Error 1

gmake: *** [ctio1gards] Error 1

#

turn off pgroute

#

[-f guards/nopgroute] || touch guards/nopgroute # # use padtiles # [-f guards/usepadtiles] || touch guards/usepadtiles # # use pifpack # [-f guards/usepifpack] || touch guards/usepifpack # # insert an instance of the clock tree # [-f guards/addclock] || touch guards/addclock # # disable old dcell placement obstruction # [-f guards/noobs] || touch guards/noobs # # now do it . . .

#

gmake GARDS_DISPLAY=clio:0.0 guards/ctio0-iter

gmake[1]: Entering directory

~/N/auspex/root/s10/chip/euterpe/verilog/bsrc/ctio'

gmake[1]: `guards/ctio0-iter' is up to date.

gmake[1]: Leaving directory

~/N/auspex/root/s10/chip/euterpe/verilog/bsrc/ctio'

#

turn off pgroute

#

[-f guards/nopgroute] || touch guards/nopgroute # # use padtiles # [-f guards/usepadtiles] || touch guards/usepadtiles # # use pifpack # [-f guards/usepifpack] || touch guards/usepifpack # # insert an instance of the clock tree # [-f guards/addclock] || touch guards/addclock # # disable old dcell placement obstruction # [-f guards/noobs] || touch guards/noobs # # now do it . . .

#

gmake GARDS_DISPLAY=clio:0.0 guards/ctio1-iter

gmake[1]: Entering directory

~/N/auspex/root/s10/chip/euterpe/verilog/bsrc/ctio'

#

Get an initial sdl file. A manhattan approximation will be used # gmake

GARDS_DISPLAY=clio:0.0 CYCLETIME=895 guards/ctio1-pass2.sdl

gmake[2]: Entering directory

~/N/auspex/root/s10/chip/euterpe/verilog/bsrc/ctio'

gmake[2]: Leaving directory

```
`/N/auspex/root/s10/chip/euterpe/verilog/bsrc/ctio'  
gmake[1]: Leaving directory  
`/N/auspex/root/s10/chip/euterpe/verilog/bsrc/ctio'  
[finished at Fri Sep 30 14:08:35 PDT 1994 -- exit status 1]
```

From: vant [vanthof@hestia]
Sent: Friday, September 30, 1994 4:13 PM
To: 'Geert Rosseel'
Cc: 'Dave Van't Hof'; 'Tim B. Robinson'; 'Alan Corry'; 'Brian Lee'; 'Mark Hofmann'
Subject: Re: path

Geert Rosseel writes:

>
>
> /n/auspex/s33/agc/euterpe/verilog/bsrc/nb/gards
>
>Geert
>

Ahhh. I found the problem in the nb section. Topt relies (heavily) on the stats information for cell area. It chooses the smallest area cell cell which meets the timing requirements.

In the case you pointed out to me, topt first finds a 2s cell which meets the timing (nice small size of 3 atoms). Topt continues on it's search to see if it can find a smaller cell which still meets timing. Well, it does eventually find a cell; xbor3df24s! That's because there is no atoms information and the size defaults to 0, which according to modern mathematics is significantly less than 3 :-)

We really need atoms information to get topt to work correct.
Dave

--
Dave Van't Hof vanthof@microunity.com MicroUnity Systems Engineering,
Inc.
"What rolls down stairs, alone or in pairs, rolls over the neighbor's dog?"

What's great for a snack and fits on your back? It's log, log, log!"
LOG from BLAMMO! (tm) All kids love Log! #include
<std_disclaim.h>

From: Buffalo Chip [chip@gamorra]
Sent: Friday, September 30, 1994 4:24 PM
To: 'geert@gamorra'
Subject: output of euterpe/verilog/bsrc/ctio/checkoutrc

Fri Sep 30 14:23:56 PDT 1994 (geert Fri, 30 Sep 1994 14:06:23 -0700)
euterpe/verilog/bsrc/ctio
[Release BOM (V19.0) in euterpe/verilog/bsrc/ctio (Fri Sep 30 14:23:57 PDT 1994)]

Dir euterpe/verilog/bsrc/ctio BOM 19.0

7.3 .checkoutrc
1.8 Makefile
10.3 clean-request
1.3 ctio.V
3.1 ctio.ut
11.2 ctio1_control.pim
3.1 ctiotester.V
3.1 ctiotester.h
1.2 ctrasel.pla
3.1 ctwasel.pla
3.1 ctwe.Veqn
9.3 genpim0.pl
9.3 genpim1.pl
13.5 genptab.pl
5.8 pimlib.pl

==> running euterpe/verilog/bsrc/ctio/.checkoutrc (Fri Sep 30 14:24:03 PDT 1994) <==

gmake: `clean' is up to date.

gmake[2]: *** No rule to make target `gards/ctio1-pass2.sdl'. Stop.

gmake[1]: *** [ctio1-base.netcap] Error 1

gmake: *** [ctio1gards] Error 1

#

turn off pgroute

#

[-f guards/nopgroute] || touch guards/nopgroute # # use padtiles # [-f guards/usepadtiles] || touch guards/usepadtiles # # use pifpack # [-f guards/usepifpack] || touch guards/usepifpack # # insert an instance of the clock tree # [-f guards/addclock] || touch guards/addclock # # disable old dcell placement obstruction # [-f guards/noobs] || touch guards/noobs # # now do it . . .

#

gmake GARDS_DISPLAY=clio:0.0 guards/ctio0-iter

gmake[1]: Entering directory

~/N/auspex/root/s10/chip/euterpe/verilog/bsrc/ctio'

gmake[1]: `guards/ctio0-iter' is up to date.

gmake[1]: Leaving directory

~/N/auspex/root/s10/chip/euterpe/verilog/bsrc/ctio'

#

turn off pgroute

#

[-f guards/nopgroute] || touch guards/nopgroute # # use padtiles # [-f guards/usepadtiles] || touch guards/usepadtiles # # use pifpack # [-f guards/usepifpack] || touch guards/usepifpack # # insert an instance of the clock tree # [-f guards/addclock] || touch guards/addclock # # disable old dcell placement obstruction # [-f guards/noobs] || touch guards/noobs # # now do it . . .

#

gmake GARDS_DISPLAY=clio:0.0 guards/ctio1-iter

gmake[1]: Entering directory

~/N/auspex/root/s10/chip/euterpe/verilog/bsrc/ctio'

#

Get an initial sdl file. A manhattan approximation will be used # gmake

GARDS_DISPLAY=clio:0.0 CYCLETIME=895 guards/ctio1-pass2.sdl

gmake[2]: Entering directory

~/N/auspex/root/s10/chip/euterpe/verilog/bsrc/ctio'

gmake[2]: Leaving directory

```
`/N/auspex/root/s10/chip/euterpe/verilog/bsrc/ctio'  
gmake[1]: Leaving directory  
`/N/auspex/root/s10/chip/euterpe/verilog/bsrc/ctio'  
[finished at Fri Sep 30 14:24:20 PDT 1994 -- exit status 1]
```

From: sysadm@gaea on behalf of Guillermo A. Loyola [gmo@microunity.com]
Sent: Friday, September 30, 1994 4:35 PM
To: 'euterpe@gaea'

In article <199409301550.IAA22270@aphrodite.microunity.com>, tbr@aphrodite.microunity.com (Tim B. Robinson) writes:

|>
|> We will implement this using bit 61 of cerberus octlet 6 (defined as
|> the unimplemented self test bit),

Although unimplemented in Euterpe, the TSA description of the selftest bit seems to imply that it would be a hardware function that results in a reset. Are we abandoning the concept completely?

Gmo.

From: Buffalo Chip [chip@rhea]
Sent: Friday, September 30, 1994 5:05 PM
To: 'geert@rhea'
Subject: pager log message

page from chip to geert:

Release euterpe/verilog/bsrc/mc BOM 26.0 initiated by dickson completed @ Fri Sep 30
15:03:40 PDT 1994 with exit status 1.. chip

From: craig
Sent: Friday, September 30, 1994 6:23 PM
To: 'gmo@microunity.com'
Cc: 'euterpe'
Subject: self-test on Euterpe

Self-test isn't part of the current implementation, and this use of bit 61 is implementation-dependent. The functionality of bit 61 is a subset of the functionality I'd like to have via the Cerberus indirect address access: the comprehensive ability to read and write all memory-mapped facilities of Euterpe. I'd do that before implementing a self-test.

Craig

From: tbr
Sent: Friday, September 30, 1994 6:33 PM
To: 'vant'
Cc: 'Geert Rosseel'; 'Mark Hofmann'; 'Lisa Robinson'; 'Dave Van't Hof'; 'Tom Vo'
Subject: lvs mismatches in xbc01df4s?
Follow Up Flag: Follow up
Flag Status: Red

vant wrote (on Fri Sep 30):

Hi, I believe I've found one reason why the fullchip euterpe lvs didn't work. The XBC01DF4S cell does not pass LVS. There are several devices missing from the layout:

```
NUMBER OF UN-MATCHED SCHEMATICS DEVICES  =  5
NUMBER OF UN-MATCHED LAYOUT  DEVICES    =  2
NUMBER OF  MATCHED SCHEMATICS DEVICES    =  1
NUMBER OF  MATCHED LAYOUT  DEVICES       =  1
```

I heard hallway talk about the C01 cells being regenerated, is this one of the repercussions? I guess the leaf cells need to be regenerated? Until they are, there is not a very good reason for running fullchip lvs's.

Sounds like we need som automation to run lvs as part of the process of generating these so we know right away if a change breaks something.

Tim

From: Tim B. Robinson [tbr@aphrodite]
Sent: Friday, September 30, 1994 6:33 PM
To: 'vant'
Cc: 'Geert Rosseel'; 'Mark Hofmann'; 'Lisa Robinson'; 'Dave Van't Hof'; 'Tom Vo'
Subject: lvs mismatches in xbc01df4s?

vant wrote (on Fri Sep 30):

Hi, I believe I've found one reason why the fullchip euterpe lvs didn't work. The XBC01DF4S cell does not pass LVS. There are several devices missing from the layout:

NUMBER OF UN-MATCHED SCHEMATICS DEVICES	=	5
NUMBER OF UN-MATCHED LAYOUT DEVICES	=	2
NUMBER OF MATCHED SCHEMATICS DEVICES	=	1
NUMBER OF MATCHED LAYOUT DEVICES	=	1

I heard hallway talk about the C01 cells being regenerated, is this one of the repercussions? I guess the leaf cells need to be regenerated?

Until they are, there is not a very good reason for running fullchip lvs's.

Sounds like we need som automation to run lvs as part of the process of generating these so we know right away if a change breaks something.

Tim

From: vant [vanthof@hestia]
Sent: Friday, September 30, 1994 6:35 PM
To: 'Tim B. Robinson'
Cc: 'geert@hestia'; 'hopper@hestia'; 'lisar@hestia'; 'vo@hestia'; 'Thomas Laidig'
Subject: Re: lvs mismatches in xbc01df4s?

Tim B. Robinson writes:

>
>
>vant wrote (on Fri Sep 30):
>
>
> Hi, I believe I've found one reason why the fullchip euterpe lvs
didn't
> work. The XBC01DF4S cell does not pass LVS. There are several
devices missing
> from the layout:
>
>
> NUMBER OF UN-MATCHED SCHEMATICS DEVICES = 5
> NUMBER OF UN-MATCHED LAYOUT DEVICES = 2
> NUMBER OF MATCHED SCHEMATICS DEVICES = 1
> NUMBER OF MATCHED LAYOUT DEVICES = 1
>
> I heard hallway talk about the C01 cells being regenerated, is this
one of
> the repercussions? I guess the leaf cells need to be regenerated?
Until
> they are, there is not a very good reason for running fullchip lvs's.
>
>Sounds like we need som automation to run lvs as part of the process of
>generating these so we know right away if a change breaks something.
>
>Tim
>

Well, usually Tom L. does this when he generates the new layouts, but since he's out this week, and the C01 generators changed, the verification wasn't possible. In general, I don't think we have a problem with new leaf cells.

Dave

--
Dave Van't Hof vanthof@microunity.com MicroUnity Systems Engineering,
Inc.

"What rolls down stairs, alone or in pairs, rolls over the neighbor's dog?"

What's great for a snack and fits on your back? It's log, log, log!"
LOG from BLAMMO! (tm) All kids love Log! #include
<std_disclaim.h>

From: lisa
Sent: Friday, September 30, 1994 7:59 PM
To: 'Jeff Marr'
Cc: 'gmo'
Subject: Re: itag bits 12:11

> I spoke with gmo about this, and I think there was a little confusion.

Nay, a *lot* of confusion. ;-) I've got a terpsichore architecture spec, a tag layout posted by tim to muse.euterpe, another posted by jay (but seemingly describing only the dtag, though it is not specific) and a micro-architecture spec which nicely numbers the bits but does not name many of them. Out of all that documentation, only Jay's and the uarch's description of the dtag protection field matches.

> In the itag, bits 13:0 are the protection field. Bits 13:12 will
> likely be implemented, and the others (11:0) will not.

Did you really mean 13:0 and 13:12 ??? Your last mail was asking about bits 12:11. Also, the uarch does say that bits 12 and 11 cause an exception if set. It also says that those 2 bits are copied directly from the gtlb protection field. The gtlb description says that bit 12 causes an exception if set, and bit 11 is ignored. If bit 12 is set in the gtlb, and causes an exception, how/when does it get copied into the itag? And is bit 11 ignored on translation, but copied to the itag, where it can then cause an exception? (If so, I wouldn't exactly call that "ignored".)

> In the dtag, bits 13:6 are part of the tag, since the dcache is tagged
> by the physical address. They have nothing to do with the index.
> Bits 5:0 are the protection field. Bits 5:4 and 0 are implemented.

Yup. Much less confusion here.

Okay. I will implement whatever you like, as long as you tell me, EXACTLY, what that is -- especially:

- Which bits mean what?
- If a bit is described as "causes an exception if set", which exception?
- If a bit is described as "ignored by the hardware", does that mean it *is* or *isn't* expected to be the same when read as it was when written?

thanks,
lisa

.

From: tbr
Sent: Friday, September 30, 1994 10:34 PM
To: 'abbott'
Subject: forwarded message from tbr
Follow Up Flag: Follow up
Flag Status: Red

resending

----- Start of forwarded message -----

To: craig
cc: euterpe
Subject: GTLB access

We have run into a problem with the GTLB mask field. When the LTLB was changed to implement only the XOR field, craig wanted the sense of the mask field inverting so that the LTLB mask would be read only with a value of 0 rather than all 1's. To be consistent with this, the GTLB definition was to be changed too, with the thinking being that all we had to do was reverse the sense of the data going in and out via the CMOS read/write ports. However, the GTLB physical array uses the same I/O pins for the mask and match arrays, effectively selecting between them with an additional address bit. So we cannot invert one without inverting the other unless we add more logic which we can ill afford in order to invert the data selectively.

I therefore propose that we go back to the original (and less confusing) definition, with the LTLB match field reading back always all 1's and no extra inversions in the GTLB path. I think this can still be justified as consistent with the general definition of reserved fields always reading zero, because this is not really a reserved field. It is the LTLB match field, which in this implementation happens to have a reserved *value* of all 1's which you can't change.

Comments please - and remember atoms are at stake!

Tim

----- End of forwarded message -----

.

From: tbr
Sent: Friday, September 30, 1994 10:34 PM
To: 'abbott'
Subject: forwarded message from tbr
Follow Up Flag: Follow up
Flag Status: Red

Resending

----- Start of forwarded message -----

To: euterpe
cc: tbr, bobm
Subject: debugger interrupt support

There has been a strong request to be able to cause an event in euterpe from an external Cerberus master to support bringup and debug. We will implement this using bit 61 of cerberus octlet 6 (defined as the unimplemented self test bit), which assignment has craig's blessing. Setting this bit will result in bit 1 of the event register being set. Acknowledging this event will require rewriting Cerberus octlet 6 to clear the bit there before clearing bit 1 in the event register.

When not required to support debug in this way (ie assuming bit 61 in octlet 6 is always 0), bit 1 of the event register can be used for normal interrupts from Calliope.

Tim

----- End of forwarded message -----

.

From: tbr
Sent: Friday, September 30, 1994 10:41 PM
To: 'vant'
Cc: 'Alan Corry'; 'Brian Lee'; 'Geert Rosseel'; 'Mark Hofmann'; 'Dave Van't Hof'
Subject: Re: path
Follow Up Flag: Follow up
Flag Status: Red

vant wrote (on Fri Sep 30):

Geert Rosseel writes:

```
>  
>  
> /n/auspex/s33/agc/euterpe/verilog/bsrc/nb/gards  
>  
>Geert  
>
```

Ahhh. I found the problem in the nb section. Topt relies (heavily) on the stats information for cell area. It chooses the smallest area cell which meets the timing requirements.

In the case you pointed out to me, topt first finds a 2s cell which meets the timing (nice small size of 3 atoms). Topt continues on it's search to see if it can find a smaller cell which still meets timing. Well, it does eventually find a cell; xbor3df24s! That's because there is _no_ atoms information and the size defaults to 0, which according to modern mathematics is significantly less than 3 :-)

We really need atoms information to get topt to work correct.

Was a warning being generated. Would it be worth having the default be a big number instead so cells with missing data would not be chosen.

I agree in general we need ALL information to be present and accurate.

Tim

From: Tim B. Robinson [tbr@aphrodite]
Sent: Friday, September 30, 1994 10:41 PM
To: 'vant'
Cc: 'Alan Corry'; 'Brian Lee'; 'Geert Rosseel'; 'Mark Hofmann'; 'Dave Van't Hof'
Subject: Re: path

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